

## SECTION 3

### ANALOG SIGNAL PROCESSING CIRCUITS

- Dynamic Range Compression
- Logarithmic Amplifiers
- Analog Multipliers
- RMS to DC Converters
- Modulators and Mixers
- Automatic Gain Control (AGC) and Voltage-Controlled Amplifiers (VCAs)



## SECTION 3

## ANALOG SIGNAL PROCESSING CIRCUITS

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## DYNAMIC RANGE COMPRESSION

In some cases, a wide dynamic range is an essential aspect of a signal, something to be preserved at all costs. This is true, for example, in the high-quality reproduction of music. However, it is often necessary to compress the signal to a smaller range without any significant loss of information. Compression is often used in magnetic recording, where the upper end of the dynamic range is limited by tape saturation, and the lower end by the granularity of the medium. In professional noise-reduction systems, compression is “undone” by precisely-matched nonlinear expansion during reproduction. Similar techniques are often used in conveying speech over noisy channels, where the performance is more likely to be measured in terms of word-intelligibility than audio fidelity. The reciprocal processes of compressing and expanding are implemented using “compandors”, and many schemes have been devised to achieve this function.

Logarithmic amps find wide applications where signals having wide dynamic ranges (perhaps greater than 100dB) must be processed by elements, such as ADCs, which may have more limited dynamic ranges. Log amps have maximum incremental gain for small signals; the gain decreases in inverse proportion to the magnitude of the input. This permits the amplifier to accept signals with a wide input dynamic range and compress them substantially.

Log amps provide nonlinear dynamic range compression and are used in applications where low harmonic distortion is not a requirement. All types of log amps produce a low dynamic range output without the need to first acquire some measure of the signal amplitude for use in controlling gain.

There is another class of *linear* dynamic range compression systems where the gain of the amplifiers in the signal processing chain is independent of the instantaneous amplitude of the signal, but is controlled by a closed loop system in such a way as to render the output (that is the peak, or rms value) essentially constant. The harmonic distortion is relatively low. These systems use what are often called *variable-gain amplifiers*. While correct, this lacks precision, because *nonlinear* amplifiers (such as log amps) also exhibit variable gain, but in direct response to the signal magnitude. The term *voltage controlled amplifier* (VCA) is preferred in this context; it clearly describes the way in which the gain control is implemented, while allowing latitude in regard to the actual circuit means used to achieve the function. The gain may be controlled by a *current* within the circuit, but usually a voltage. Analog multipliers may be used as VCAs, but other topologies will also be discussed later in this section.

In this section, we will first examine *nonlinear* signal compression using log amps. A discussion of analog multipli-

ers follows, with emphasis on analog signal processing applications. Finally, a discussion of *linear* compression techniques using voltage-controlled

amplifiers within automatic-gain-control (AGC) loops concludes the section.

### LOGARITHMIC AMPLIFIERS

The term "Logarithmic Amplifier" (generally abbreviated to "log amp") is something of a misnomer, and "Logarithmic Converter" would be a better description. The conversion of a signal to its equivalent logarithmic value involves a nonlinear operation, the consequences of which can be confusing if not fully understood. It is important to realize that many of the familiar concepts of linear circuits are irrelevant to log amps. For example, the incremental gain of an ideal log amp approaches infinity as the input tends to zero, and a change of offset at the output of a log amp is equivalent to a change of amplitude at its input - not a change of input offset.

For the purposes of simplicity in our initial discussions, we shall assume that

both the input and the output of a log amp are voltages, although there is no particular reason why logarithmic current, transimpedance, or transconductance amplifiers should not also be designed.

If we consider the equation  $y = \log(x)$  we find that every time  $x$  is multiplied by a constant  $A$ ,  $y$  increases by another constant  $A1$ . Thus if  $\log(K) = K1$ , then  $\log(AK) = K1 + A1$ ,  $\log(A^2K) = K1 + 2A1$ , and  $\log(K/A) = K1 - A1$ . This gives a graph as shown in Figure 3.1, where  $y$  is zero when  $x$  is unity,  $y$  approaches minus infinity as  $x$  approaches zero, and which has no values for  $x$  for which  $y$  is negative.

### GRAPH OF $Y = \text{LOG}(X)$

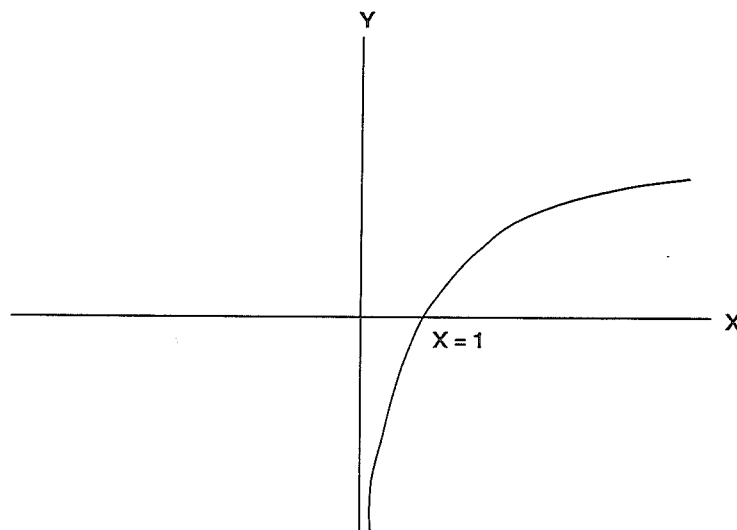


Figure 3.1

On the whole, log amps do not behave in this way. Apart from the difficulties of arranging infinite negative output voltages, such a device would not, in fact, be very useful. A log amp must satisfy a transfer function of the form

$$V_{\text{out}} = V_y \log(V_{\text{in}}/V_x)$$

over some range of input values which may vary from 100:1 (40dB) to over 1,000,000:1 (120dB).

With inputs very close to zero, log amps cease to behave logarithmically, and most then have a linear  $V_{\text{in}}/V_{\text{out}}$  law. This behavior is often lost in device noise. Noise often limits the dynamic

range of a log amp. The constant,  $V_y$ , has the dimensions of voltage, because the output is a voltage. The input,  $V_{\text{in}}$ , is divided by a voltage,  $V_x$ , because the argument of a logarithm must be a simple dimensionless ratio.

A graph of the transfer characteristic of a log amp is shown in Figure 3.2. The scale of the horizontal axis (the input) is logarithmic, and the ideal transfer characteristic is a straight line. When  $V_{\text{in}} = V_x$ , the logarithm is zero ( $\log 1 = 0$ ).  $V_x$  is therefore known as the *intercept voltage* of the log amp because the graph crosses the horizontal axis at this value of  $V_{\text{in}}$ .

## LOG AMP TRANSFER FUNCTION

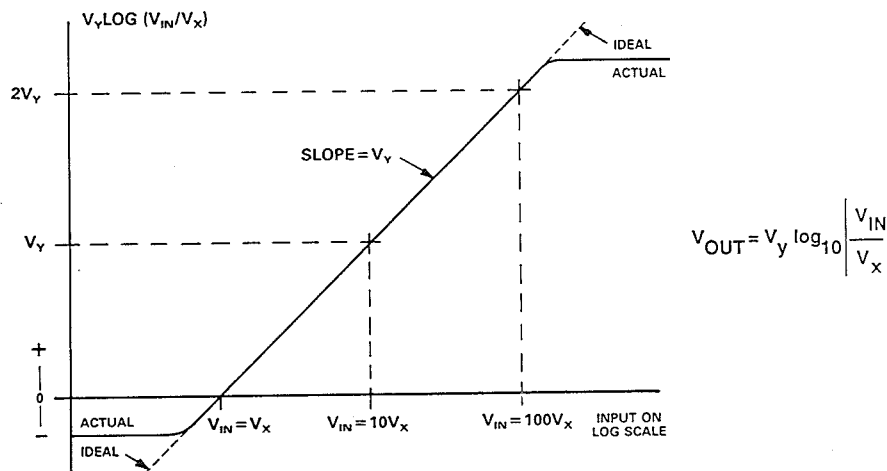


Figure 3.2

The slope of the line is proportional to  $V_y$ . When setting scales, logarithms to the base 10 are most often used because this simplifies the relationship to decibel values: when  $V_{in} = 10V_x$ , the logarithm has the value of 1, so the output voltage is  $V_y$ . When  $V_{in} = 100V_x$ , the output is  $2V_y$ , and so forth.  $V_y$  can therefore be viewed either as the "slope voltage" or as the "volts per decade factor."

The logarithm function is indeterminate for negative values of  $x$ . Log amps can respond to negative inputs in three different ways: (1) They can give a fullscale negative output as shown in

Figure 3.3. (2) They can give an output which is proportional to the log of the absolute value of the input and disregards its sign as shown in Figure 3.4. This type of log amp can be considered to be a full-wave detector with a logarithmic characteristic, and is often referred to as a *detecting* log amp. (3) They can give an output which is proportional to the log of the absolute value of the input and has the same sign as the input as shown in Figure 3.5. This type of log amp can be considered to be a video amp with a logarithmic characteristic, and may be known as a *logarithmic video* (*log video*) amplifier or, sometimes, a *true log amp*.

### BASIC LOG AMP (SATURATES WITH NEGATIVE INPUT)

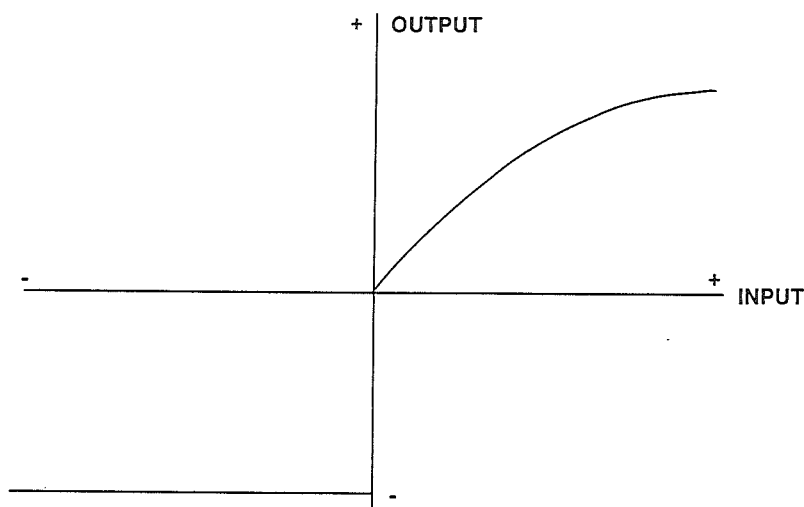


Figure 3.3

**DETECTING LOG AMP  
(OUTPUT POLARITY INDEPENDENT  
OF INPUT POLARITY)**

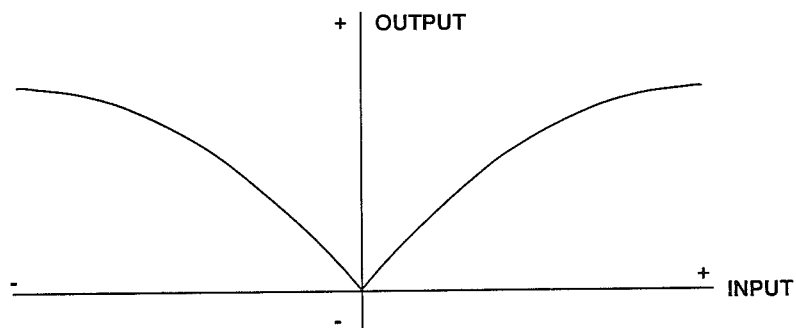


Figure 3.4

**LOG VIDEO OR "TRUE LOG AMP"  
(SYMMETRICAL RESPONSE  
TO POSITIVE OR NEGATIVE SIGNALS)**

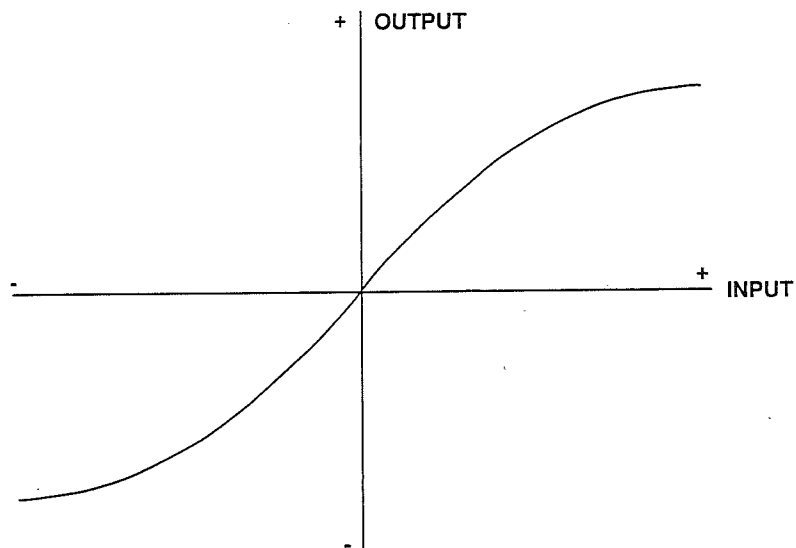


Figure 3.5

There are three basic architectures which may be used to produce log amps: the *basic diode log amp*, the *successive detection log amp*, and the "true log amp" which is based on cascaded semi-limiting amplifiers.

The voltage across a silicon diode is proportional to the logarithm of the current through it. If a diode is placed in the feedback path of an inverting op-amp, the output voltage will be proportional to the log of the input current as shown in Figure 3.6. In practice, the dynamic range of this configuration is limited to 40-60dB because of non-ideal diode characteristic, but if the diode is replaced with a diode-connected transistor as shown in Figure 3.7, the dynamic range can be extended to 120dB or more. This type of log amp has three disadvantages: (1) both the slope and intercept are temperature dependent; (2) it will only handle unipolar signals; and (3) its bandwidth is both limited

and dependent on signal amplitude. Where several such log amps are used on a single chip to produce an analog computer which performs both log and antilog operations, the temperature variation in the log operations is unimportant, since it is compensated by a similar variation in the antilogging. This makes possible the AD538, a monolithic analog computer which can multiply, divide, and raise to powers (see Figure 3.8). Where actual logging is required, however, the AD538 and similar circuits require temperature compensation (Reference 7). The major disadvantage of this type of log amp for high frequency applications, though, is its limited frequency response - which cannot be overcome. However carefully the amplifier is designed, there will always be a residual feedback capacitance  $C_c$  (often known as Miller capacitance), from output to input which limits the high frequency response (See Figure 3.7).

## THE DIODE / OP-AMP LOG AMP

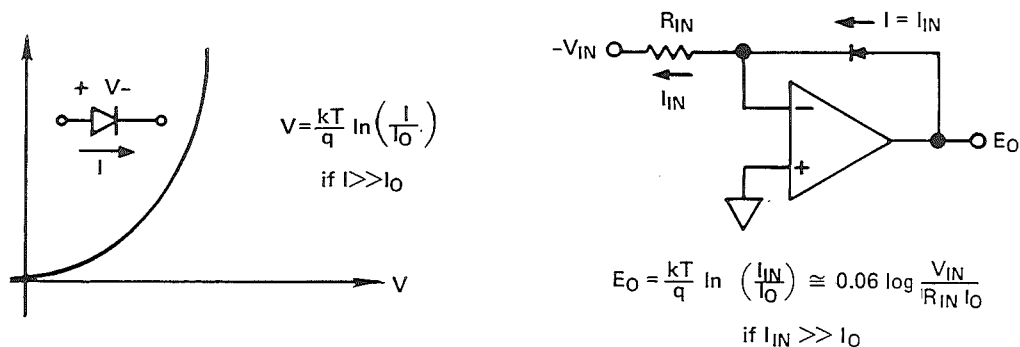


Figure 3.6



## TRANSISTOR / OP-AMP LOG AMP

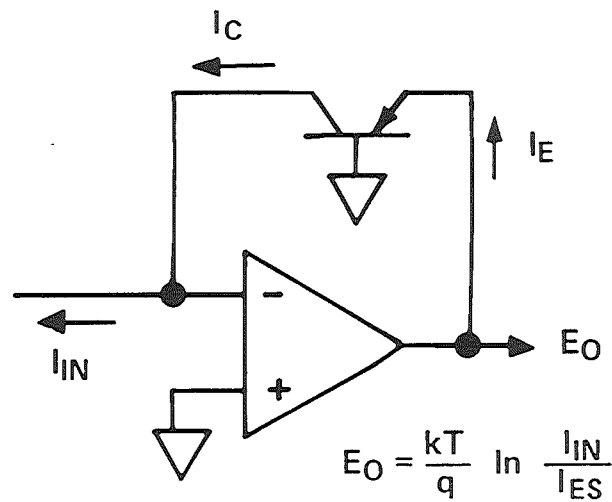


Figure 3.7

## AD538 LOG AMP SIMPLIFIED DIAGRAM

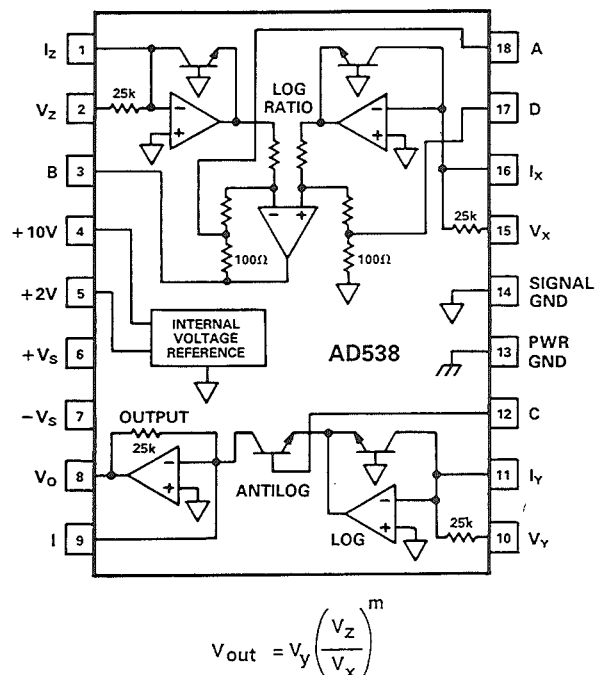


Figure 3.8

What makes this Miller capacitance particularly troublesome is that the impedance of the emitter-base junction is inversely proportional to the current flowing in it - so that if the log amp has a dynamic range of 1,000,000:1, then its bandwidth will also vary by 1,000,000:1. In practice, the variation is less because other considerations limit the large signal bandwidth, but it is very difficult to make a log amp of this type with a small-signal bandwidth greater than a few hundred kHz.

For high frequency applications, therefore, detecting and "true log" architectures are used. Although these differ in detail, the general principle behind

their design is common to both: instead of one amplifier having a logarithmic characteristic, these designs use a number of similar cascaded linear stages having well-defined large signal behavior.

Consider N cascaded limiting amplifiers, the output of each driving a summing circuit as well as the next stage (Figure 3.9). If each amplifier has a gain of A dB, the small signal gain of the strip is NA dB. If the input signal is small enough for the last stage not to limit, the output of the summing amplifier will be dominated by the output of the last stage.

## BASIC MULTI-STAGE LOG AMP ARCHITECTURE

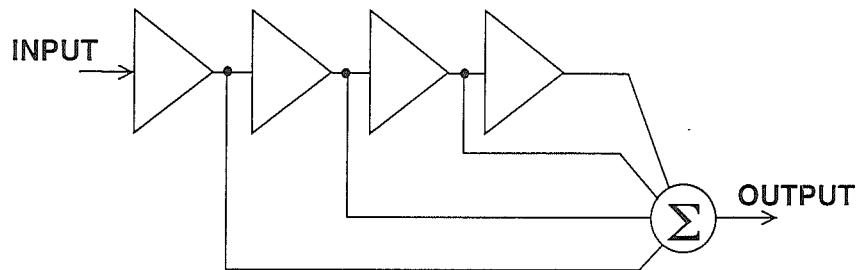


Figure 3.9

As the input signal increases, the last stage will limit. It will now make a fixed contribution to the output of the summing amplifier, but the incremental gain to the summing amplifier will drop to  $(N-1)A$  dB. As the input continues to increase, this stage in turn will limit and make a fixed contribution to the output, and the incremental gain will drop to  $(N-2)A$  dB, and so forth - until the first stage limits, and the output ceases to change with increasing signal input.

The response curve is thus a set of straight lines as shown in Figure 3.10. The total of these lines, though, is a very good approximation to a logarithmic curve, and in practical cases, is an even better one, because few limiting amplifiers, especially high frequency ones, limit quite as abruptly as this model assumes.

### BASIC MULTI-STAGE LOG AMP RESPONSE (UNIPOLAR CASE)

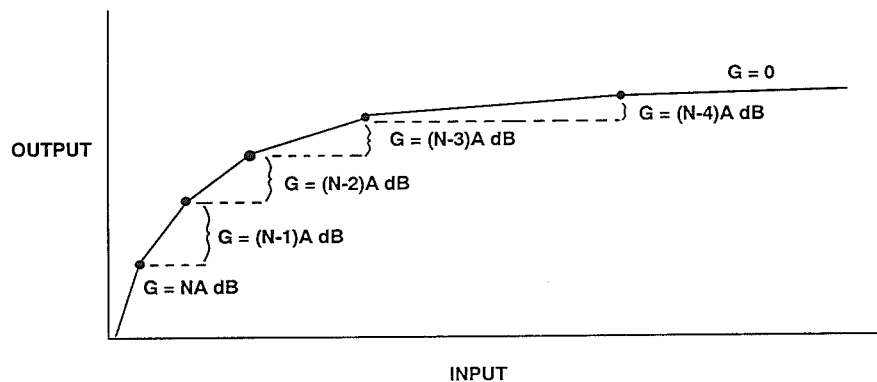


Figure 3.10

The choice of gain,  $A$ , will also affect the log linearity. If the gain is too high, the log approximation will be poor. If it is too low, too many stages will be required to achieve the desired dynamic range. Generally, gains of 10 to 12 dB ( $3x$  to  $4x$ ) are chosen.

This is, of course, an ideal and very general model - it demonstrates the

principle, but its practical implementation at very high frequencies is difficult. Assume that there is a delay in each limiting amplifier of  $t$  nanoseconds (this delay may also change when the amplifier limits but let's consider first order effects!). The signal which passes through all  $N$  stages will undergo delay of  $Nt$  nanoseconds, while the signal which only passes one stage will be

delayed only  $t$  nanoseconds. This means that a small signal is delayed by  $Nt$  nanoseconds, while a large one is "smeared", and arrives spread over  $Nt$  nanoseconds. A nanosecond equals a foot at the speed of light, so such an effect represents a spread in position of  $Nt$  feet in the resolution of a radar system-which may be unacceptable in some systems (for most log amp applications this is not a problem).

A solution is to insert delays in the signal paths to the summing amplifier, but this can become complex. Another solution is to alter the architecture slightly so that instead of limiting gain stages, we have stages with small

signal gain of  $A$  and large signal (incremental) gain of unity (0dB). We can model such stages as two parallel amplifiers, a limiting one with gain, and a unity gain buffer, which together feed a summing amplifier as shown in Figure 3.11.

Figure 3.11 shows that such stages, cascaded, form a log amp without the necessity of summing from individual stages. Both the multi-stage architectures described above are *video* log amplifiers, or *true log* amplifiers, but the most common type of high frequency log amplifier is the *successive detection* log amp architecture shown in Figure 3.12.

## STRUCTURE AND PERFORMANCE OF "TRUE" LOG AMP ELEMENT AND OF A LOG AMP FORMED BY SEVERAL SUCH ELEMENTS

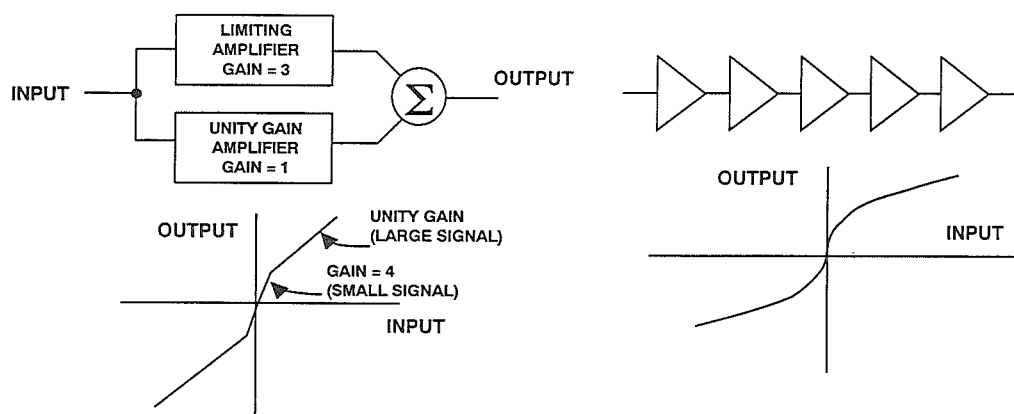
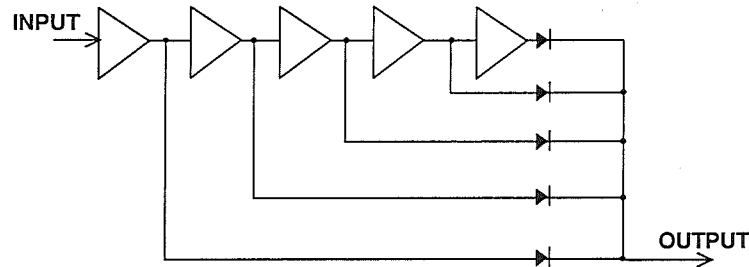


Figure 3.11

## SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER



Detectors may be full- or half-wave but should be current output devices (not simple diodes) so that the detector outputs may be summed without additional summing components being necessary.

Figure 3.12

The *successive detection* log amp consists of cascaded limiting stages as described above, but instead of summing their outputs directly, these outputs are applied to detectors, and the detector outputs are summed as shown in Figure 3.12. If the detectors have current outputs, the summing process may involve no more than connecting all the detector outputs together.

Log amps using this architecture have two outputs: the log output and a limiting output. In many applications, the limiting output is not used, but in some (FM receivers with “S”-meters, for example), both are necessary.

The log output of a successive detection log amplifier generally contains ampli-

tude information, and the phase and frequency information is lost. This is not necessarily the case, however, if a half-wave detector is used, and attention is paid to equalizing the delays from the successive detectors - but the design of such log amps is demanding.

The specifications of log amps will include *noise*, *dynamic range*, *frequency response* (some of the amplifiers used as successive detection log amp stages have low frequency as well as high frequency cutoff), the *slope of the transfer characteristic* (which is expressed as V/dB or mA/dB depending on whether we are considering a voltage- or current-output device), the *intercept point* (the input level at which the output voltage or current is zero), and the *log linearity*. (See Figures 3.13 and 3.14)

## KEY PARAMETERS OF LOG AMPS

- **NOISE:** The Noise Referred to the Input (RTI) of the Log Amp. It May Be Expressed as a Noise Figure or as a Noise Spectral Density (Voltage, Current, or Both) or as a Noise Voltage, a Noise Current, or Both
- **DYNAMIC RANGE:** Range of Signal Over Which the Amplifier Behaves in a Logarithmic Manner (Expressed in dB)
- **FREQUENCY RESPONSE:** Range of Frequencies Over Which the Log Amp Functions Correctly
- **SLOPE:** Gradient of Transfer Characteristic in V/dB or mA/dB
- **INTERCEPT POINT:** Value of Input Signal at Which Output is Zero
- **LOG LINEARITY:** Deviation of Transfer Characteristic (Plotted on log/lin Axes) from a Straight Line (Expressed in dB)

Figure 3.13

## LOG LINEARITY

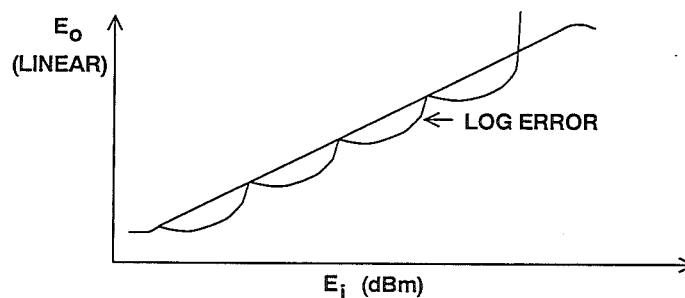


Figure 3.14

In the past, it has been necessary to construct high performance, high frequency successive detection log amps (called log strips) using a number of individual monolithic limiting amplifiers such as the one shown in Figure

3.15). Notice that such components are not, themselves, log amps but are components from which log amps may be made. The circuit contains a limiting amplifier which drives both the output and an internal half-wave rectifier.

### SIMPLIFIED SCHEMATIC OF MONOLITHIC LIMITING AMPLIFIER WITH HALF-WAVE DETECTOR (SL-1521)

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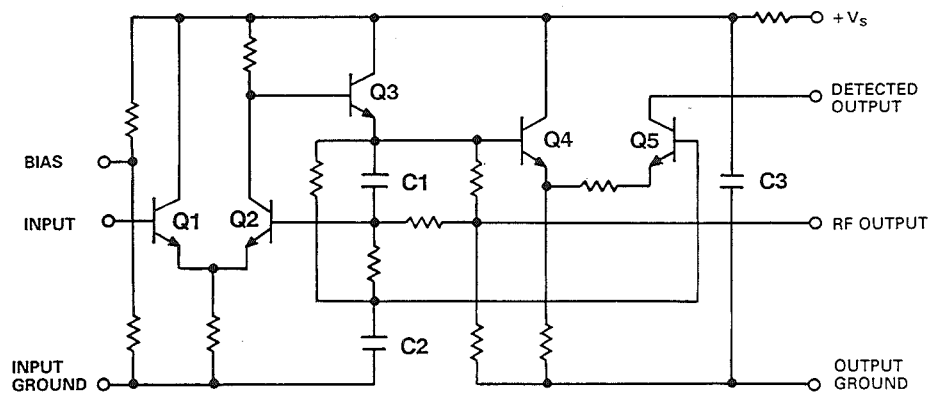


Figure 3.15

### PERFORMANCE OF LIMITING / DETECTING AMPLIFIER (SL-1521)

- Bandwidth: 7MHz to 245MHz
- Voltage Gain: 12dB
- Maximum Detected Output Current: 1mA at 60MHz, RF Input = 0.5V rms
- Maximum RF Output Voltage: 1.6V peak-to-peak
- Maximum Input Before Overload: 1.9V rms
- Power Dissipation: 84mW

Figure 3.16

Figure 3.17 shows the overall transfer function of a log amp made with four such stages. The detected current output of each stage is plotted against input, as is the sum of all the outputs.

It is clear that the sum of these currents approximates a straight line for inputs between  $300\mu\text{V}$  and  $100\text{mV}$  - about 48dB.

### 4-STAGE SUCCESSIVE DETECTION LOG STRIP CONSTRUCTED FROM LIMITING / DETECTING AMPLIFIERS (SL-1521s)

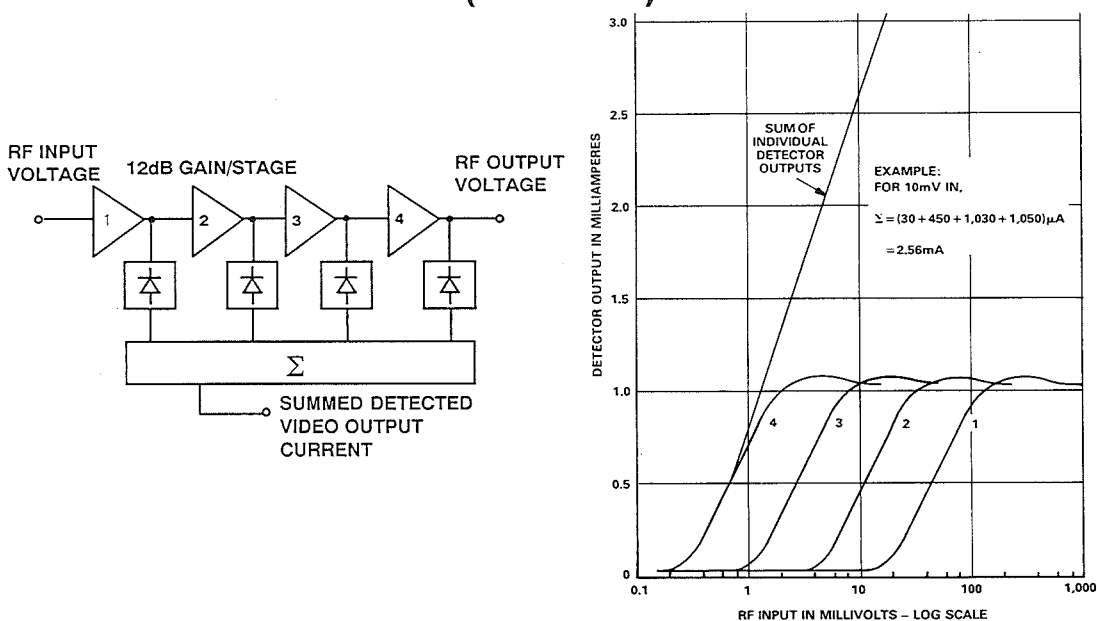


Figure 3.17

If we add stages, the dynamic range increases by 12 dB with each stage until the strip limits on the noise of its own input stage. This occurs with six stages if they are simply connected together broadband. If the noise figure is 5dB at  $450\Omega$ , this gives about  $70\mu\text{V}$  broadband noise (assuming 220MHz bandwidth). The limiting amplifier limits with 100mV drive, so there must be a gain of less than 1428 (63dB) to the input of the last stage. At 12dB/stage, this requires five stages so, with the output stage, we cannot have more than six stages without limiting on noise. This gives a dynamic range of less than 70dB.

We can increase the dynamic range by placing an interstage filter between the third and fourth stages of the strip to limit the bandwidth as shown in Figure 3.18. If we reduce the bandwidth to 10MHz, the noise is reduced by the square root of 22 (13.5dB), so we are still limited to seven stages. The interstage filter used does not affect the accuracy of the log response, PROVIDED that it has a voltage gain which is precisely unity throughout the pass-band.



## 105 dB LOG AMP USING AN AUXILIARY STRIP (SL-1521s)

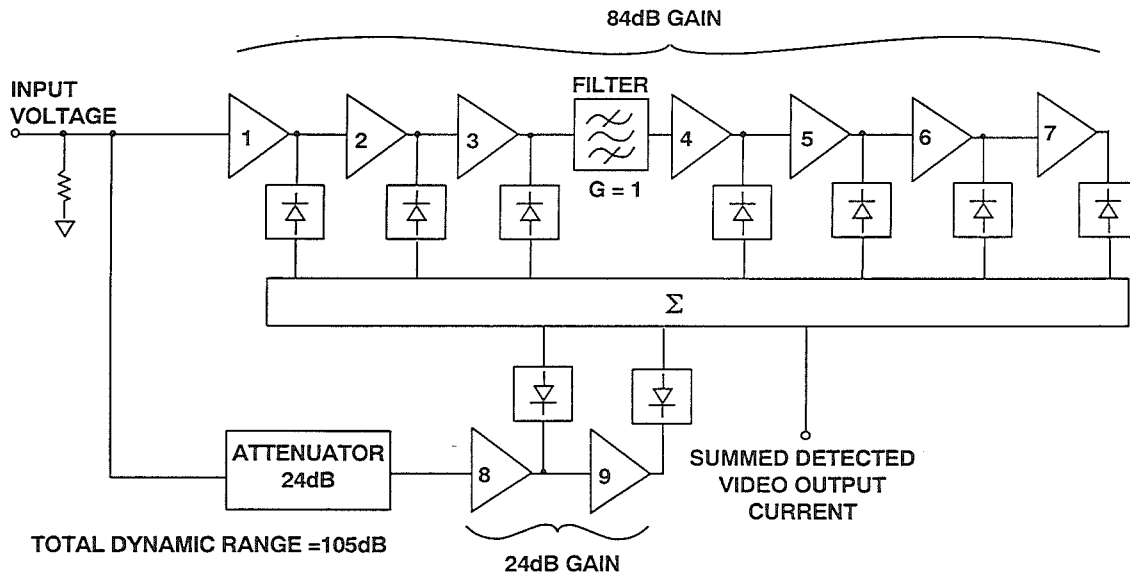


Figure 3.18

If we allow for the effects of noise, seven stages will only give some 80dB dynamic range. If further dynamic range is required, we must use an auxiliary strip. This makes use of the fact that although the output of the limiting amplifier saturates with 100mV input, the device operates without problems with inputs up to 1.9V.

If, therefore, we add another two stage strip of limiting amplifiers, with a 24dB attenuator at its input, in parallel with the existing strip, and summing its outputs to those of the existing strip, we can add another 24dB of detector range before the input to the main seven-stage strip is overloaded. This gives us nine stages, for a theoretical dynamic range of 108dB - in practice, it is possible to achieve about 103-105dB.

When constructing a log strip such as the one described above, there are

various considerations of coupling, decoupling, filter design, and feedback via the detector pins which must be addressed in any successful design. The single stage limiting amplifier building block has a low frequency cutoff of about 10MHz which makes it impossible to use in many lower frequency applications.

Recent advances in IC processes have allowed the complete log strip function to be integrated into a single chip, thereby eliminating the need for costly hybrid log strips.

The AD640 log amp contains five limiting stages (10dB per stage) and five full-wave detectors in a single IC package, and its logarithmic performance extends from dc to 145MHz. Furthermore, its amplifier and full-wave detector stages are balanced so that, with reasonably well-considered layout,

instability from feedback via supply rails is unlikely. A block diagram of the AD640 is shown in Figure 3.19. Unlike all previous integrated circuit log amps, the AD640 is laser trimmed to high absolute accuracy of both slope and

intercept, and is fully temperature compensated. Key features of the AD640 are summarized in Figure 3.20. The transfer function for the AD640 as well as the log linearity is shown in Figure 3.21.

## BLOCK DIAGRAM OF THE AD640 MONOLITHIC LOG AMP

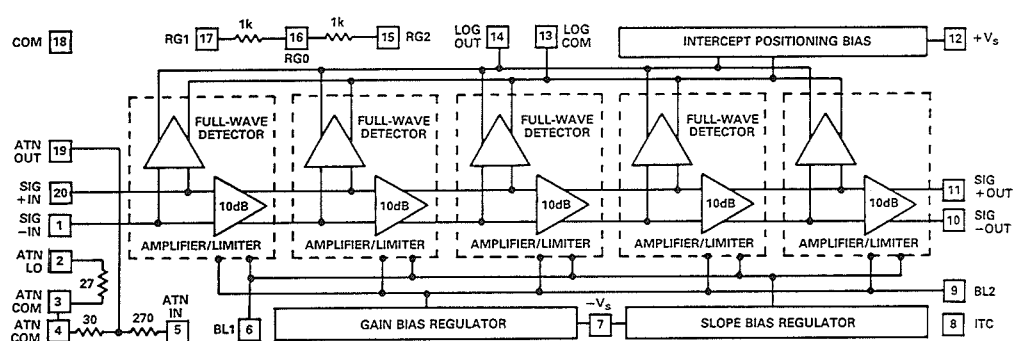


Figure 3.19

## AD640 KEY FEATURES

- 45dB Dynamic Range - Two AD640s Cascadable to 95dB
- Bandwidth dc to 145MHz - 120MHz when Cascaded
- Laser-Trimmed Slope of 1mA/decade - Temperature Stable
- Laser-Trimmed Intercept of 1mV - Temperature Stable
- Less than 1dB Log Non-Linearity
- Balanced Circuitry for Stability
- Minimal External Component Requirement

Figure 3.20

## DC LOGARITHMIC TRANSFER FUNCTION AND ERROR CURVE FOR SINGLE AD640

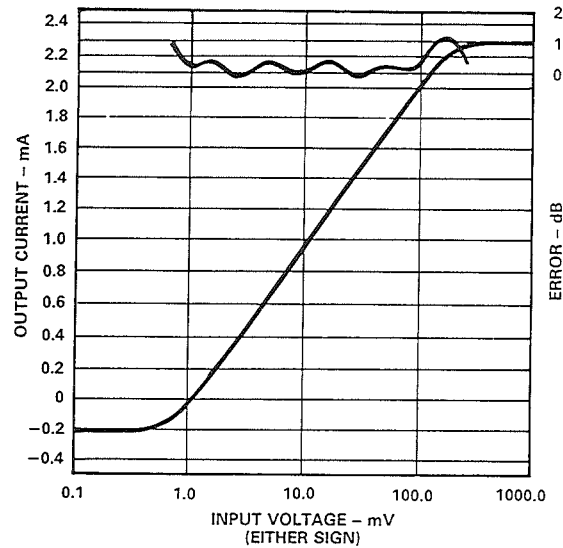


Figure 3.21

Because of its high accuracy, the actual waveform driving the AD640 must be considered when calculating responses. When a waveform passes through a log function generator, the mean value of

the resultant waveform changes. This does not affect the slope of the response, but the apparent intercept is modified according to Figure 3.22.

## THE EFFECT OF WAVEFORM ON INTERCEPT POINT

INPUT WAVEFORM	PEAK OR RMS	INTERCEPT FACTOR	ERROR (RELATIVE TO A DC INPUT)
Square Wave	Either	1	0.00dB
Sine Wave	Peak	2	-6.02dB
Sine Wave	RMS	$1.414 (\sqrt{2})$	-3.01dB
Triwave	Peak	$2.718 (e)$	-8.68dB
Triwave	RMS	$1.569 (e/\sqrt{3})$	-3.91dB
Gaussian Noise	RMS	1.887	-5.52dB

Figure 3.22

The AD640 is calibrated and laser trimmed to give its defined response to a DC level or a symmetrical 2kHz square wave. It is also specified to have an intercept of 2mV for a sinewave input (that is to say a 2kHz sinewave of amplitude 2mV peak [not peak-to-peak] gives the same mean output signal as a DC or square wave signal of 1mV).

The waveform also affects the ripple or nonlinearity of the log response. This ripple is greatest for DC or square wave inputs because every value of the input

voltage maps to a single location on the transfer function, and thus traces out the full nonlinearities of the log response. By contrast, a general time-varying signal has a continuum of values within each cycle of its waveform. The averaged output is thereby "smoothed" because the periodic deviations away from the ideal response, as the waveform "sweeps over" the transfer function, tend to cancel. As is clear in Figure 3.23, this smoothing effect is greatest for a triwave.

## THE EFFECT OF WAVEFORM ON AD640 LOG LINEARITY AND INTERCEPT POINT

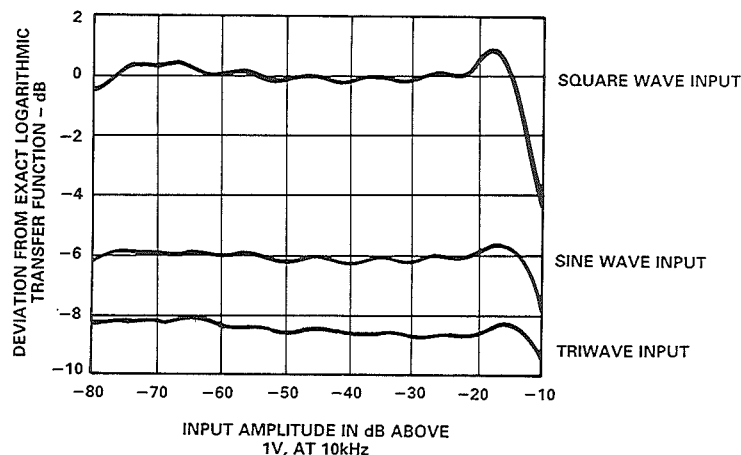


Figure 3.23

Each of the five stages in the AD640 has a gain of 10dB and a full-wave detected output. The transfer function for the device was shown in Figure 3.21 along with the error curve. Note the excellent log linearity over an input range of 1 to 100mV (40dB). Although well suited to RF applications, the AD640 is dc-coupled throughout. This allows it to be used in LF and VLF

systems, including audio measurements, sonar, and other instrumentation applications requiring operation to low frequencies or even dc.

When two AD640s are cascaded, the second will be delivering an output from the noise of the first. If the full potential dynamic range is to be realized, the bandwidth must be limited. This may

be done with high-pass, low-pass, or band-pass filters, depending on the required response, but the voltage gain of these filters in their passband must be unity, or there will be a kink in the log response. Figure 3.24 shows a 70dB log amp for broadband operation from

50 to 150MHz. The 100MHz passband limits the possible dynamic range, but the performance is still exceptional. Figure 3.25 shows a 95dB 10Hz to 100kHz log amp using two cascaded AD640s.

### 70dB LOG AMP FOR 50-150MHz USING TWO AD640s

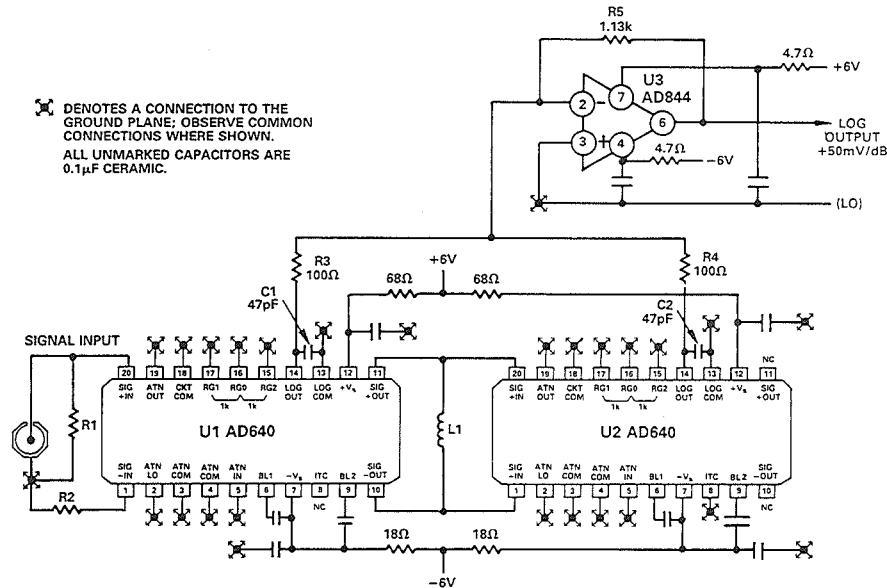


Figure 3.24

### 95dB LOW FREQUENCY LOG AMP (10Hz - 100kHz) USING TWO AD640s

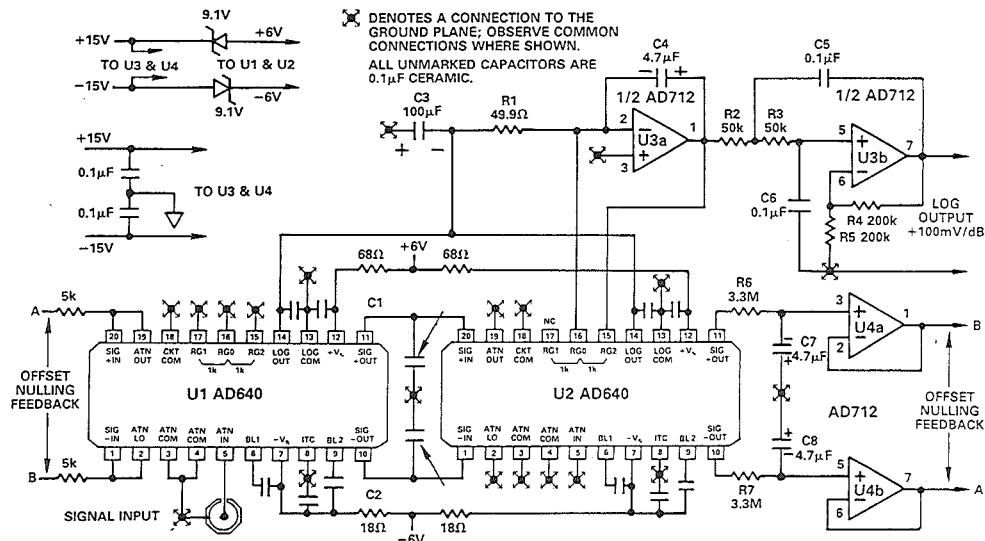


Figure 3.25

An external op amp can be used to convert the AD640 output current to a buffered output voltage as shown in Figure 3.26. The input to the AD640 (1mV to 100mV, or 40dB) results in an op amp output of 0 to 2V. If this output is applied to an 8 bit flash ADC having a corresponding input range, the weight of the ADC least significant bit (LSB) is 0.157dB reflected to the input of the AD640. For input signals near zero, the

LSB value (reflected to the AD640 input) is approximately 0.02mV, while for signals approaching 100mV, the LSB value is approximately 2mV. This corresponds to an effective dynamic range of  $20\log_{10}(100\text{mV}/0.02\text{mV})$ , or 74dB. The 50dB dynamic range of the 8 bit flash converter has therefore been increased to 74dB (equivalent to a 12 bit ADC) through the use of the 40dB AD640 and the op amp.

### OP-AMP CONVERTS CURRENT OUTPUT OF AD640 TO A VOLTAGE FOR DRIVING A FLASH CONVERTER

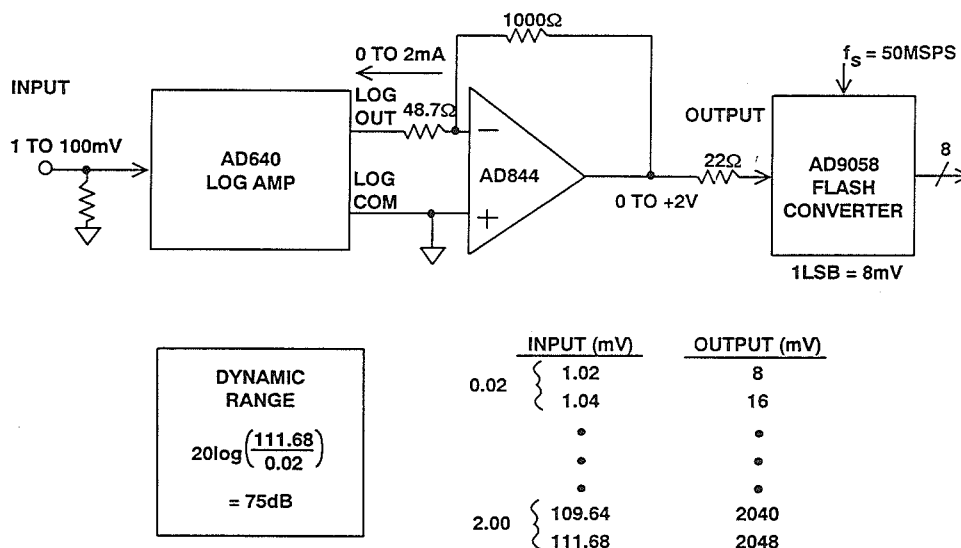


Figure 3.26

The AD606 is a complete monolithic 70MHz bandwidth log amp using 9 stages of successive detection, and is shown in Figure 3.27. Key specifications are summarized in Figure 3.28. Seven of the amplifier/detector stages handle inputs from -80dBm (32μV rms) up to about -14dBm (45mV rms). The noise floor is about -83dBm (18μV rms). Another two parallel stages receive the input attenuated by 22.3dB, and respond to inputs up to +10dBm (707mV rms). The gain of each stage is 11.15dB

and is accurately stabilized over temperature by a precise biasing system.

The AD606 provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation lowpass filter and provides an output voltage of +0.1V DC to +4V DC. The logarithmic scaling is such that the output is +0.5V for a sinusoidal input of -75dBm, and +3.5V at an input of +5dBm. Over this range, the log linearity is typically within ±0.4dB.

## AD606 50MHz, 80dB LOG AMP BLOCK DIAGRAM

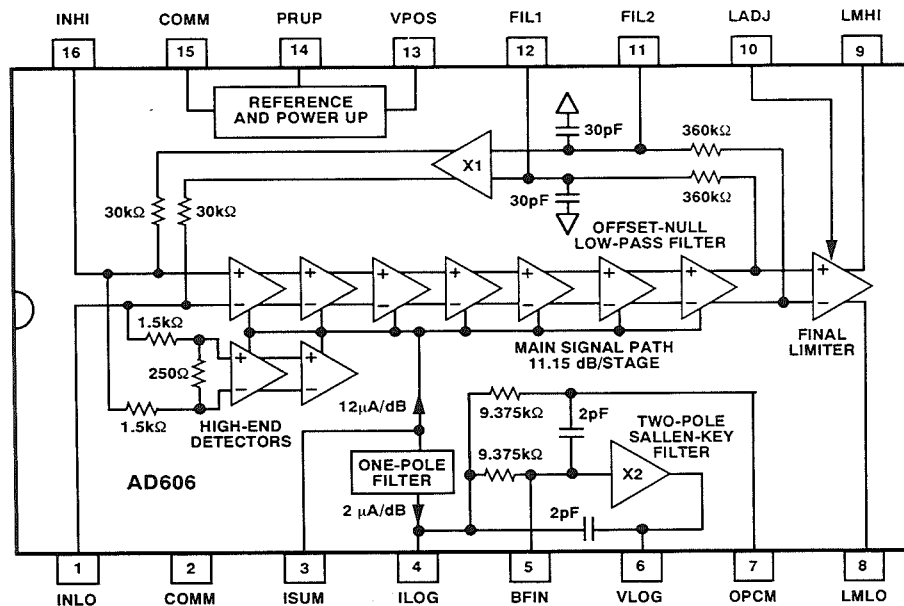


Figure 3.27

## AD606 LOG AMP KEY FEATURES

- Dynamic Range:  $-75\text{dBm}$  to  $+5\text{dBm}$  (80dB)
- Input Noise:  $< 1.5\text{nV}/\sqrt{\text{Hz}}$
- Usable from 200Hz to Greater than 50MHz
- Slope:  $37.5\text{mV/dB}$  Voltage Output
- On-Chip Lowpass Output Filter
- +5V Single-Supply, 65mW Power Consumption

Figure 3.28

The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90dB of conversion range. A second lowpass filter automatically nulls the input offset of the first stage down to the submicrovolt level.

The AD606's limiter output provides a hard-limited signal output as a differen-

tial current of  $\pm 1.2\text{mA}$  from open-collector outputs. In a typical application, both of these outputs are loaded by  $200\Omega$  resistors to provide a voltage gain of more than 90dB from the input. This limiting amplifier has exceptionally low amplitude-to-phase conversion.

## **ANALOG MULTIPLIERS**

A multiplier is a device having two input ports and an output port. The signal at the output is the product of the two input signals. If both input and output signals are voltages, the transfer characteristic is the product of the two voltages divided by a scaling factor,  $K$ , which has the dimension of voltage (see Figure 3.29). From a mathematical point of view, multiplication is a "four quadrant" operation - that is to say that both inputs may be either positive or negative, as may be the output. Some of the circuits used to produce electronic multipliers, however, are limited to signals of one polarity. If both signals must be unipolar, we have a "single quadrant" multiplier, and the output will also be unipolar. If one of the signals is unipolar, but the other may

have either polarity, the multiplier is a "two quadrant" multiplier, and the output may have either polarity (and is "bipolar"). The circuitry used to produce one- and two-quadrant multipliers may be simpler than that required for four quadrant multipliers, and since there are many applications where full four quadrant multiplication is not required, it is common to find accurate devices which work only in one or two quadrants. An example is the AD539, a wideband dual two-quadrant multiplier which has a single unipolar  $V_y$  input with a relatively limited bandwidth of 5MHz, and two bipolar  $V_x$  inputs, one per multiplier, with bandwidths of 60MHz. A block diagram of the AD539 is shown in Figure 3.31.



## BASIC ANALOG MULTIPLIER

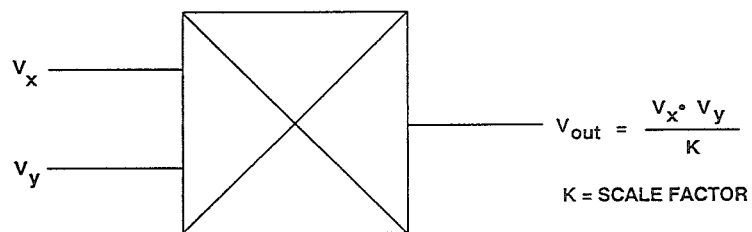


Figure 3.29

## TYPES OF MULTIPLIERS

Type	$V_x$	$V_y$	$V_{out}$
Single Quadrant	Unipolar	Unipolar	Unipolar
Two Quadrant	Bipolar	Unipolar	Bipolar
Four Quadrant	Bipolar	Bipolar	Bipolar

Figure 3.30

## AD539 FUNCTIONAL BLOCK DIAGRAM

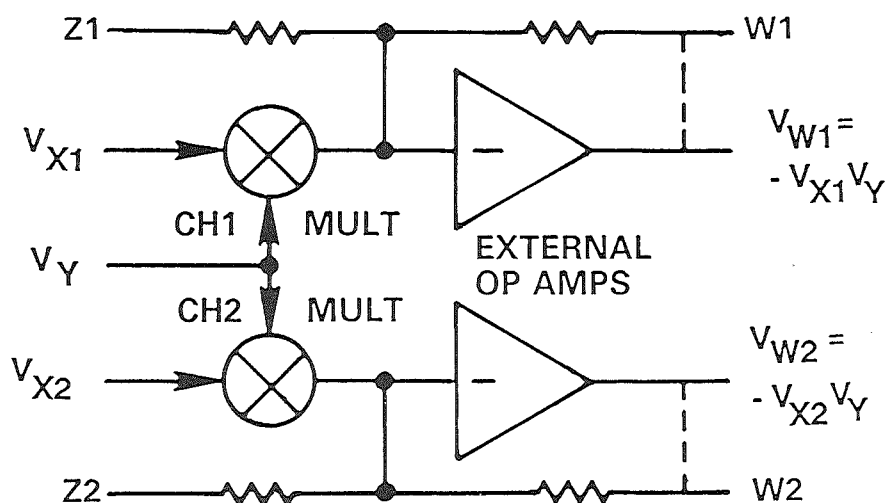


Figure 3.31

The simplest electronic multipliers use logarithmic amplifiers. The computation relies on the fact that the antilog of the

sum of the logs of two numbers is the product of those numbers (see Figure 3.32).

## COMPUTATION WITH LOG AND ANTILOG CIRCUITS

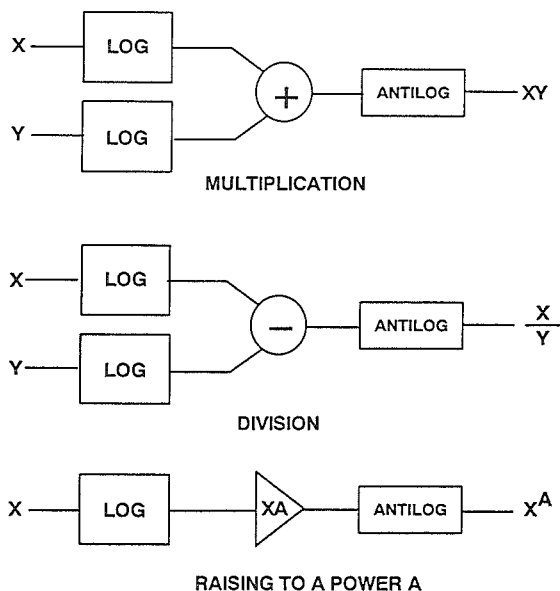


Figure 3.32

The disadvantages of this type of multiplication are the very limited bandwidth and single quadrant operation. A far better type of multiplier uses the "Gilbert Cell". This structure was invented by Barrie Gilbert in the late 1960s. (See References 1 and 2).

There is a linear relationship between the collector current of a silicon junction transistor and its transconductance (gain) which is given by

$$dI_C / dV_{be} = qI_C / kT,$$

where

$I_C$  = the collector current  
 $V_{be}$  = the base-emitter voltage  
 $q$  = the electron charge (1.60219E-19)  
 $k$  = Boltzmann's constant (1.38062E-23)  
 $T$  = the absolute temperature.

This relationship may be exploited to construct a multiplier with a long-tailed pair of silicon transistors, as shown in Figure 3.33.

This is a rather poor multiplier because (1) the Y input is offset by the  $V_{be}$  - which changes non-linearly with  $V_y$ ; (2) the X input is non-linear as a result of the exponential relationship between  $I_C$  and  $V_{be}$ ; and (3) the scale factor varies with temperature.

Gilbert realized that this circuit could be linearized and made temperature stable by working with currents, rather than voltages, and by exploiting the logarithmic  $I_C/V_{be}$  properties of transistors (See Figure 3.34.) The X input to the Gilbert Cell takes the form of a differential current, and the Y input is a unipolar current. The differential X currents flow in two diode-connected transistors, and the logarithmic voltages compensate for the exponential  $V_{be}/I_C$  relationship. Furthermore, the  $q/kT$  scale factors cancel. This gives the Gilbert Cell the linear transfer function

$$\Delta I_C = \frac{\Delta I_X I_Y}{I_X}$$

## BASIC TRANSCONDUCTANCE MULTIPLIER CIRCUIT

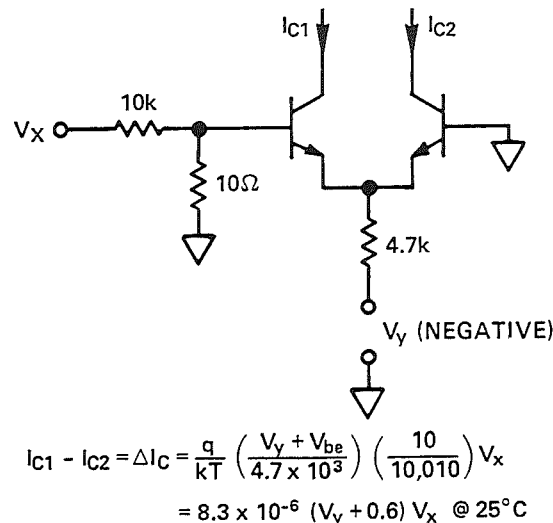
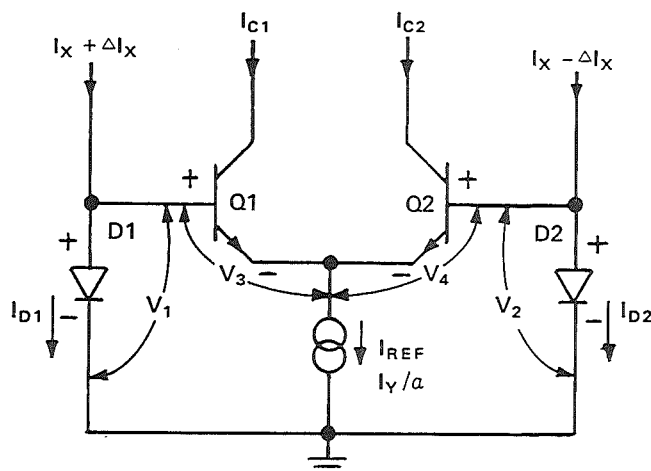


Figure 3.33

## THE GILBERT CELL: A LINEAR TWO-QUADRANT MULTIPLIER

$$\Delta I_C = I_{C1} - I_{C2}$$



$$\Delta I_C = \frac{\Delta I_X I_Y}{I_X}$$

Figure 3.34

As it stands, the Gilbert Cell has three inconvenient features: (1) its X input is a differential current; (2) its output is a differential current; and (3) its Y input is a unipolar current - so the cell is only a two quadrant multiplier.

By cross-coupling two such cells and using two voltage-to-current converters (as shown in Figure 3.35), we can convert the basic architecture to a four

quadrant device with voltage inputs, such as the AD534. At low and medium frequencies, a subtractor amplifier may be used to convert the differential current at the output to a voltage. Because of its voltage output architecture, the bandwidth of the AD534 is only about 1MHz, although the AD734, a later version, has a bandwidth of 10MHz.

## 4-QUADRANT TRANSLINEAR MULTIPLIER: THE AD534

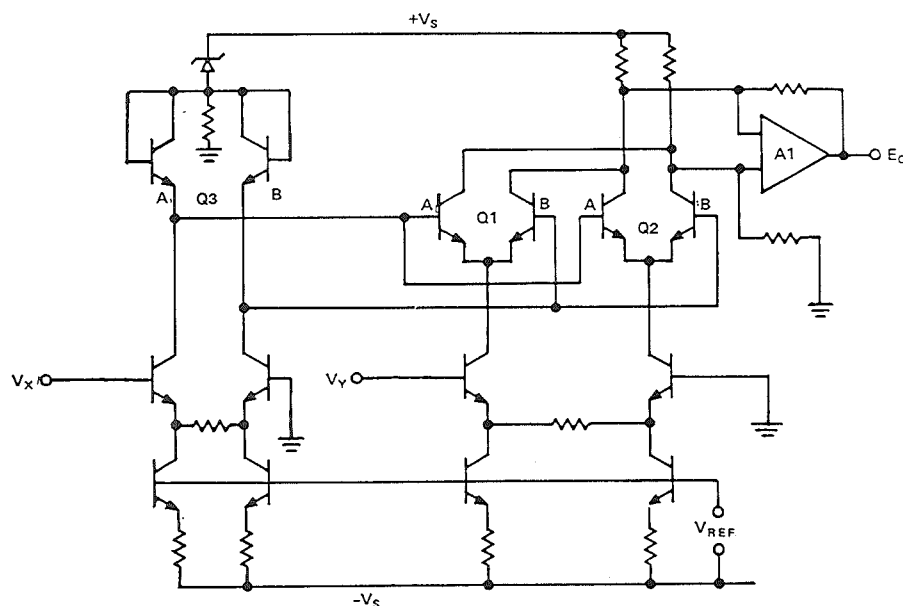


Figure 3.35

In Figure 3.35, Q1A & Q1B, and Q2A & Q2B form the two core long-tailed pairs of the two Gilbert Cells, while Q3A and Q3B are the linearizing transistors for both cells. In Figure 3.35 there is an operational amplifier acting as a differential current to single-ended voltage converter, but for higher speed applications, the cross-coupled collectors of Q1 and Q2 form a differential open collector current output (as in the AD834 500MHz multiplier).

The translinear multiplier relies on the matching of a number of transistors and currents. This is easily accomplished on a monolithic chip. Even the best IC processes have some residual errors,

however, and these show up as four dc error terms in such multipliers (see Figure 3.36). In early Gilbert Cell multipliers, these errors had to be trimmed by means of resistors and potentiometers external to the chip, which was somewhat inconvenient. With modern analog processes, which permit the laser trimming of SiCr thin film resistors on the chip itself, it is possible to trim these errors during manufacture so that the final device has very high accuracy. Internal trimming has the additional advantage that it does not reduce the high frequency performance, as may be the case with external trimpots.

### TRIMMABLE ERRORS IN MULTIPLIERS

- X-Input Offset Voltage:      Y Feedthrough
- Y-Input Offset Voltage:      X Feedthrough
- Z-Input (Output Amplifier)  
    Voltage Offset:              dc Output Offset Voltage
- Resistor Mismatch:          Gain Error

Figure 3.36

### KEY FEATURES OF THE TRANSLINEAR MULTIPLIER

- High Accuracy: Better than 0.1% Possible
- Wide Bandwidth (Over 60MHz Voltage Output, Over 500MHz Current Output)
- Simplicity, Low Cost, and Ease of Use

Figure 3.37

Because the internal structure of the translinear multiplier is necessarily differential, the inputs are usually differential as well (after all, if a single-ended input is required it is not hard to ground one of the inputs). This is not only convenient in allowing common-mode signals to be rejected, it also permits more complex computations to be performed. The AD534 (shown previously in Figure 3.35) is the classic example of a four-quadrant multiplier based on the Gilbert Cell. It has an accuracy of 0.1% in the multiplier mode,

fully differential inputs, and a voltage output. However, as a result of its voltage output architecture, its bandwidth is only about 1MHz.

For wideband applications, the basic multiplier with open collector current outputs is used. The AD834 is an 8-pin device with differential X inputs, differential Y inputs, differential open collector current outputs, and a bandwidth of over 500MHz. A block diagram is shown in Figure 3.38.

### THE AD834 FOUR-QUADRANT 500MHz MULTIPLIER

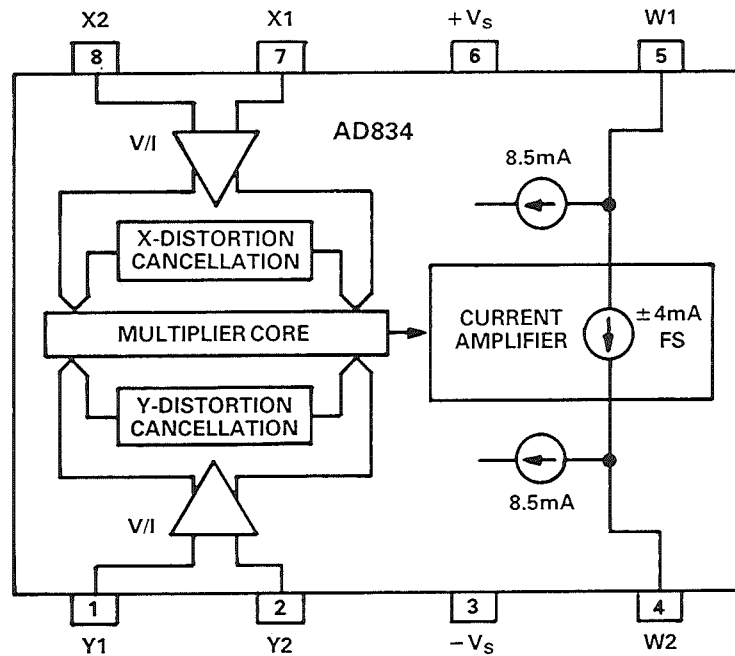


Figure 3.38

The AD834 is a true linear multiplier with a transfer function of

$$I_{out} = \frac{V_x \cdot V_y}{1V \cdot 250\Omega}$$

Its X and Y offsets are trimmed to  $500\mu V$  (3mV max), and it may be used

in a wide variety of applications including multipliers (broadband and narrowband), squarers, frequency doublers, and high frequency power measurement circuits. A consideration when using the AD834 is that, because of its very wide bandwidth, its input bias currents, approximately  $50\mu A$  per input, must be considered in the design

of input circuitry lest, flowing in source resistances, they give rise to unplanned offset voltages.

A basic wideband multiplier using the AD834 is shown in Figure 3.39. The differential output current flows in equal load resistors, R1 and R2, to give a differential voltage output. This is the simplest application circuit for the device. Where only the high frequency outputs are required, transformer coupling may be used, with either

simple transformers, or for better wideband performance, transmission line or "Ruthroff" transformers (See Reference 3).

The AD734 is a 10MHz four-quadrant multiplier with an external input to dynamically change the scale factor, thereby accomplishing a direct-divide function. A functional block diagram of the device is shown in Figure 3.41.

## BASIC CONNECTIONS FOR WIDEBAND AD834 OPERATION

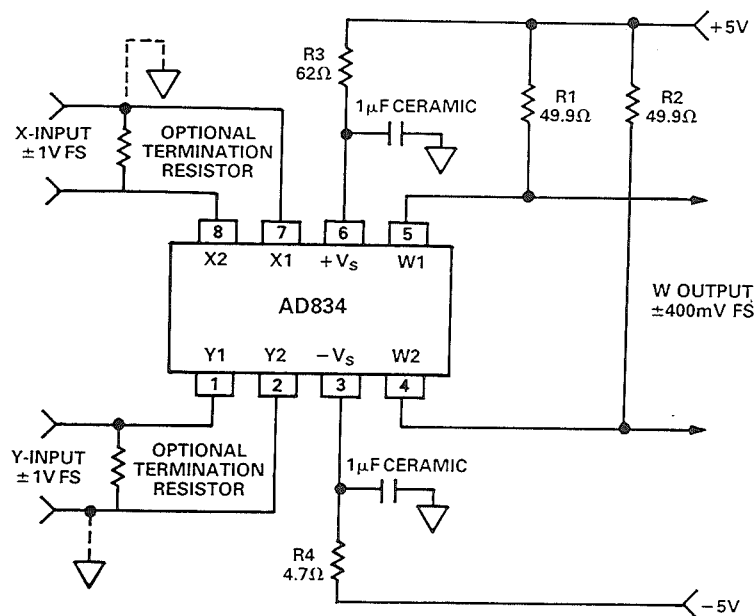


Figure 3.39



### AD834 OPERATION WITH WIDEBAND TRANSFORMER COUPLED OUTPUT

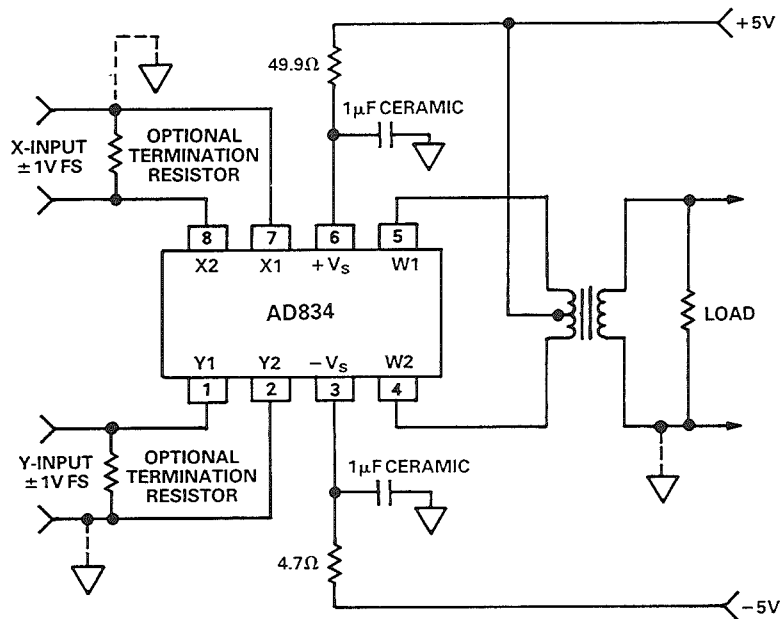
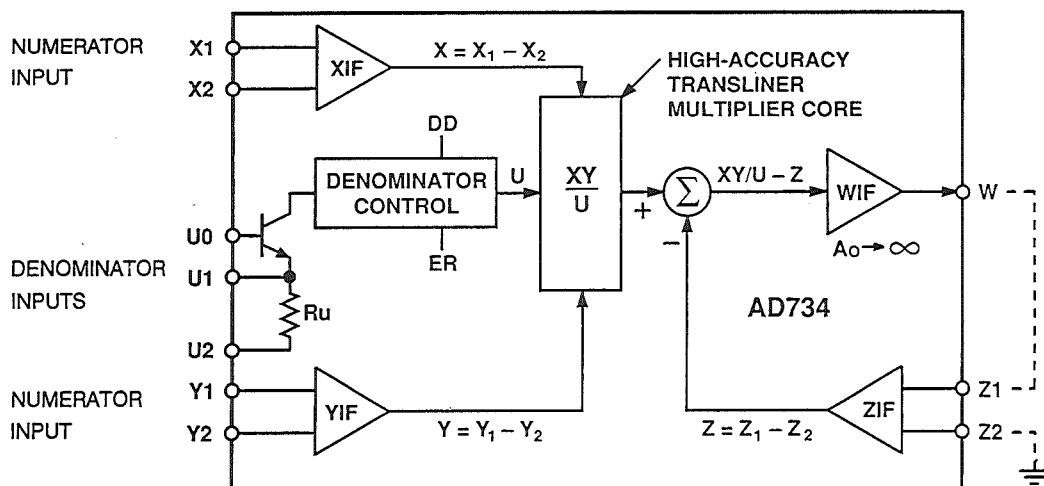


Figure 3.40

### A 10MHz MULTIPLIER WITH DIRECT-DIVIDE CAPABILITY: THE AD734



$$W = \left[ \frac{(X_1 - X_2)(Y_1 - Y_2)}{U_1 - U_2} - (Z_1 - Z_2) \right] A_0$$

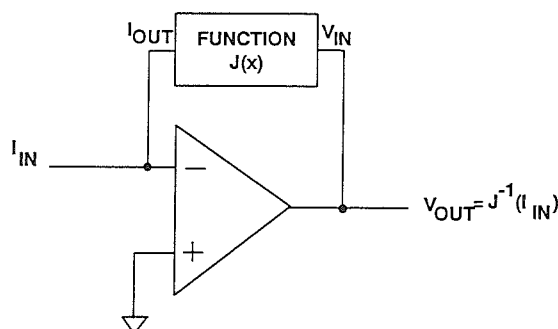
Figure 3.41

Multipliers can be placed in the feedback loop of op amps to form several useful functions. Figure 3.42 illustrates the basic principle of analog computation that a function generator in a negative feedback loop computes the

inverse function (provided, of course, that the function is monotonic over the range of operations).

Figure 3.43 shows a multiplier and an op amp configured as a divider in both inverting and non-inverting mode.

### A FUNCTION GENERATOR IN A NEGATIVE-FEEDBACK LOOP GENERATES THE INVERSE FUNCTION



NOTE: FUNCTION MUST BE MONOTONIC OVER THE RELEVANT RANGE

Figure 3.42

### MULTIPLIERS USED WITH OP-AMPS TO PERFORM DIVISION

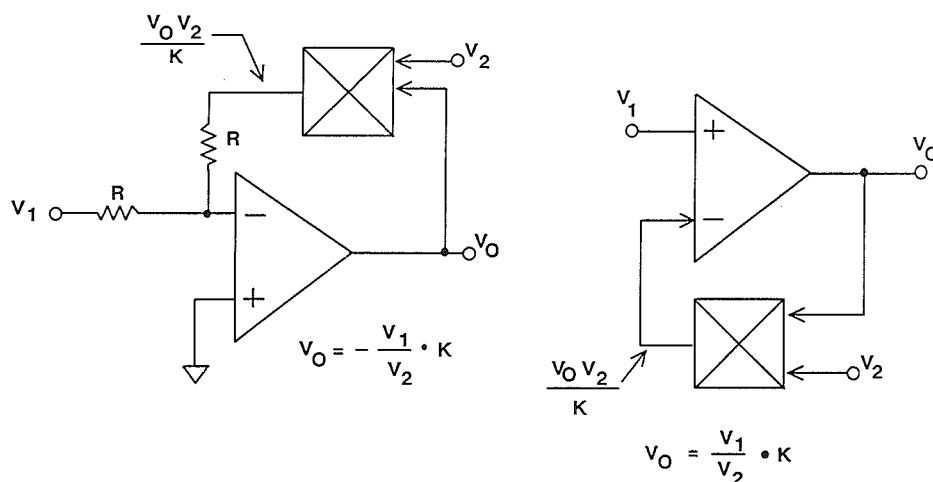


Figure 3.43

## RMS TO DC CONVERTERS

The root mean square (rms) is a fundamental measurement of the magnitude of an ac signal. Defined practically, the rms value assigned to the ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Defined mathematically, the rms value of a voltage is defined as the value obtained by squaring the signal, taking the average, and then taking the square root. The averaging time must be sufficiently long to allow filtering at the lowest frequencies of operation desired. A complete discussion of rms to dc converters can be found in Reference 13, but we will show a few examples of how efficiently analog circuits can perform this function.

The first method, called the *explicit* method, is shown in Figure 3.44. The

input signal is first squared by a multiplier. The average value is then taken by using an appropriate filter, and the square root is taken using an op amp with a second squarer in the feedback loop. This circuit has limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. This restricts this method to inputs which have a maximum dynamic range of approximately 10:1 (20dB). However, excellent bandwidth (greater than 100MHz) can be achieved with high accuracy if a multiplier such as the AD834 is used as a building block (see Figure 3.45).

3

### EXPLICIT RMS COMPUTATION

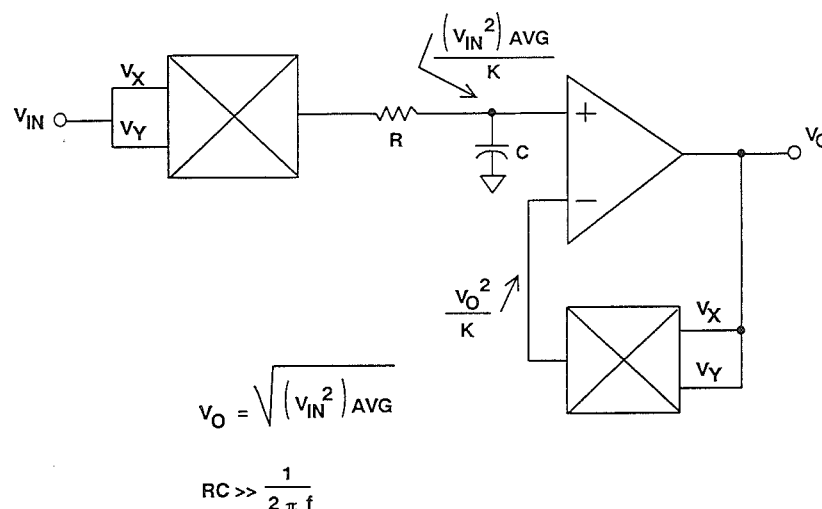


Figure 3.44

# WIDEBAND RMS MEASUREMENT WITH THE AD834

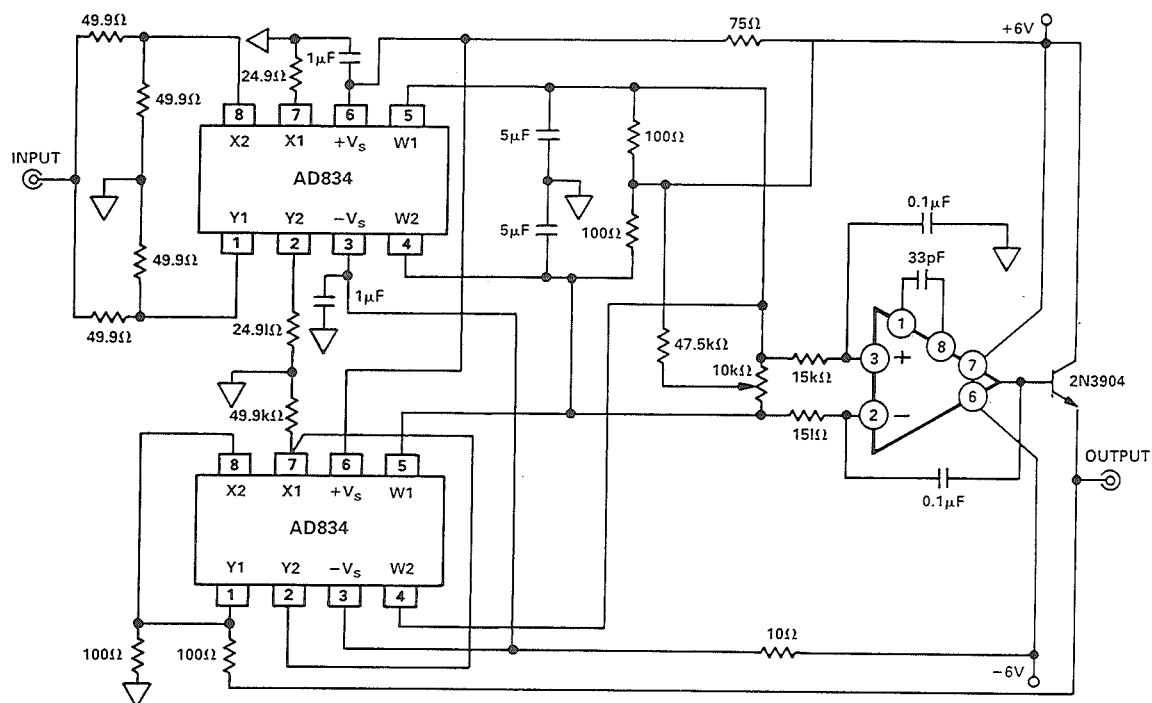


Figure 3.45

Figure 3.46 shows the circuit for computing the rms value of a signal using the *implicit* method. Here, the output is fed back to the direct-divide input of a multiplier such as the AD734. In this circuit, the output of the multiplier varies linearly (instead of as the square)

with the rms value of the input. This considerably increases the dynamic range of the implicit circuit as compared to the explicit circuit. The disadvantage of this approach is that it generally has less bandwidth than the explicit computation.

## IMPLICIT RMS COMPUTATION

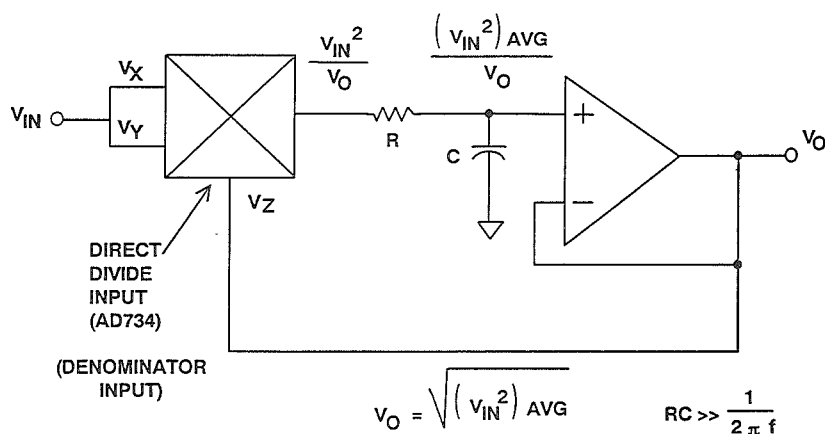


Figure 3.46

While it is possible to construct such an rms circuit from an AD734, it is far simpler to design a dedicated rms circuit. The  $V_{IN}^2/V_Z$  circuit may be current driven and need only be one quadrant if the input first passes through an absolute value circuit.

Figure 3.47 shows a simplified diagram of a typical monolithic RMS/DC converter, the AD536A. It is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage  $V_{IN}$ , which can be AC or DC, is converted to a unipolar current,  $I_1$ , by the absolute value circuit A1, A2.  $I_1$  drives one input of the one-quadrant squarer/divider which has the transfer function:  $I_4 = I_1^2/I_3$ . The output current,  $I_4$ , of the squarer/divider drives the current mirror through a lowpass filter formed by R1 and externally connected capacitor,  $C_{AV}$ . If the  $R1C_{AV}$  time constant is much greater than the longest period of the input signal, then  $I_4$  is effectively

averaged. The current mirror returns a current,  $I_3$ , which equals  $\text{AVG}[I_4]$ , back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{AVG}[I_1^2/I_4] = I_1 \text{rms}$$

The current mirror also produces the output current,  $I_{out}$ , which equals  $2I_4$ .  $I_{out}$  can be used directly or converted to a voltage with R2 and buffered by A4 to provide a low impedance voltage output. The transfer function becomes:

$$V_{out} = 2R2 \cdot I_{rms} = V_{IN} \text{ rms}$$

The dB output is derived from the emitter of Q3, since the voltage at this point is proportional to  $-\log V_{IN}$ . Emitter follower, Q5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current ( $I_{REF}$ ) to Q5 approximates  $I_3$ . However, the gain of the dB circuit has a TC of approximately 3300ppm/°C and must be temperature compensated.

## THE AD536A MONOLITHIC RMS-TO-DC CONVERTER

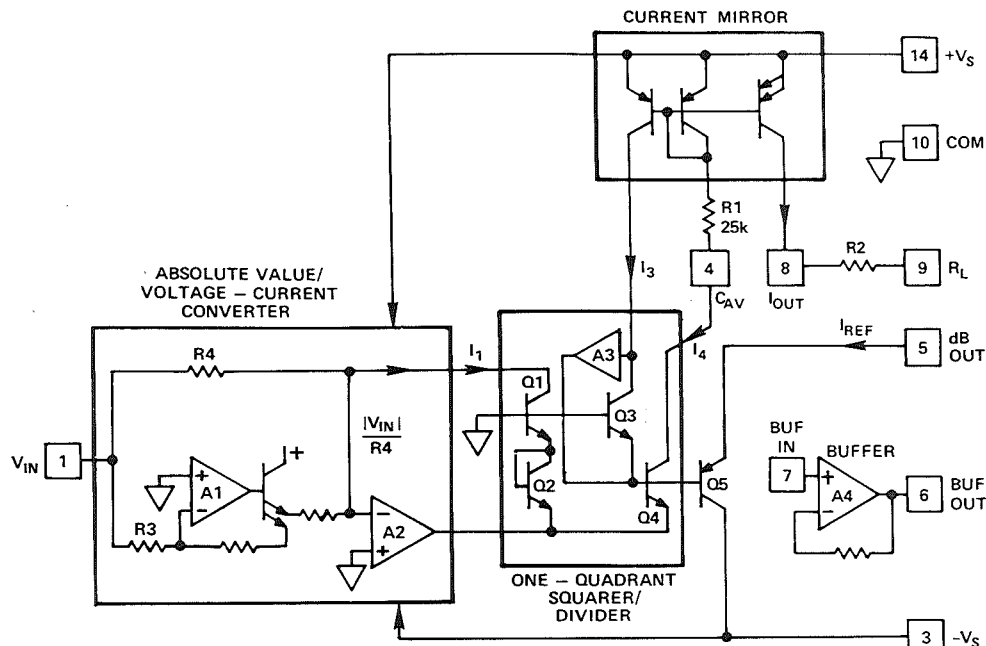


Figure 3.47

There are a number of commercially available RMS/DC converters in monolithic form which make use of these principles. The AD536A is a true RMS/DC converter with a bandwidth of approximately 450kHz for  $V_{\text{rms}} > 100\text{mV rms}$ , and 2MHz bandwidth for  $V_{\text{rms}} > 1\text{V rms}$ . The AD636 is

designed to provide 1MHz bandwidth for low-level signals up to 200mV rms. The AD637 has a 600kHz bandwidth for 100mV rms signals, and an 800MHz bandwidth for 1V rms signals. Low cost, general purpose RMS/DC converters such as the AD736 and AD737 (power-down option) are also available.

## MODULATORS AND MIXERS

A *modulator* (also called a *mixer* when it is used as a frequency changer) is closely related to a multiplier. The output of a multiplier is the instantaneous product of its inputs. The output of a modulator is the instantaneous product of a *signal* on one of its inputs (known as the *signal* input) and the *sign of the signal* on the other input (known as the *carrier* input). A modulator may be modeled as an amplifier whose gain is switched positive and negative by the output of a comparator on its carrier input (as in the case of

the AD630 balanced modulator) - or as a multiplier with a high-gain limiting amplifier between the carrier output and one of its ports (see Figure 3.48). Both architectures have been used to produce modulators, but the switched amplifier version, although potentially very accurate, tends to be rather slow. Most high speed integrated circuit modulators consist of the translinear multiplier (based on the Gilbert Cell) with a limiting amplifier in the carrier path.

### TWO MODULATOR MODELS

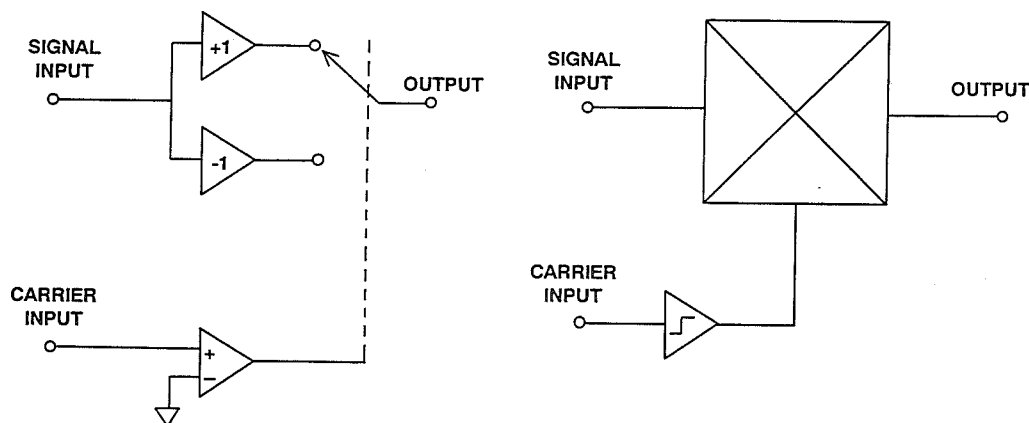


Figure 3.48

If two periodic waveforms,  $A_m \cos(\omega_m t)$  and  $A_c \cos(\omega_c t)$ , are applied to the inputs of a multiplier (with a scale factor of 1V for simplicity of analysis), then the output will be given by:

$$V_o(t) = 1/2 A_m A_c [\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t]$$

This signal contains signals at the sum and difference frequencies, but not at the original frequencies. Some RF engineers also call these the upper and lower *sidebands*. There is a 6dB loss in an ideal modulator. Note that using the cosine formulae rather than sine formulae makes the equations easier to manipulate because  $\cos(a) = \cos(-a)$  (which makes sign unimportant during

simplification), and because  $\cos(0)=1$ , so that for DC signals (when  $\omega_m t=0$ ),  $\cos(\omega_m t)$  is equal to unity.

When we say that the original frequencies are not present in the output of a modulator, we make the assumption that the modulator is perfectly balanced - i.e. neither its signal port nor its carrier port has any offset. In practice, both ports will have some offset, and so there will be some signal and carrier leakage. Trimming offset on the inputs of a modulator will reduce the leakages, but there will always be untrimmable residual leakages which are due to coupling by stray capacitance, and to nonlinearities in the core, rather than to offsets.

## CAUSES OF SIGNAL AND CARRIER LEAKAGE IN MODULATORS

- Offset on the Signal Port Causes Carrier Leakage
- Offset on the Carrier Port Causes Signal Leakage
- Even when all offsets have been trimmed out there is residual signal and carrier leakage caused by stray capacitance and core nonlinearities.

Figure 3.49

This "sum and difference mixer" is the function which we expect of modulators. However, if we use a linear multiplier as a modulator, we find that any noise or modulation on the carrier input appears in the output signal. If we replace the simple multiplier with a modulator, any amplitude variation on the carrier input disappears.

Like an analog multiplier, a modulator multiplies two signals. But unlike analog multipliers, the multiplication is not linear. Instead, the signal input is "chopped" by the local oscillator carrier signal that alternates between +1 and -1 in sign (i.e., a squarewave). This is equivalent to passing the carrier signal  $A_c \cos(\omega_c t)$  through a comparator, or limiting amplifier. The square wave with a frequency of  $\omega_c t$  has the form represented by the Fourier series of odd harmonics:

$$K[\cos(\omega_c t) - 1/3 \cos(3\omega_c t) + 1/5 \cos(5\omega_c t) - 1/7 \cos(7\omega_c t) + \dots]$$

The sum of the series:  $[1, -1/3, +1/5, -1/7 + \dots]$  is  $\pi/4$ . Therefore, the value of  $K$  is  $4/\pi$ , such that a balanced modulator acts as a unity gain amplifier when a positive DC signal is applied to its carrier input.

Therefore, if a modulator is driven by a signal  $A_m \cos(\omega_m t)$  and a carrier  $\cos(\omega_c t)$  (the carrier amplitude is unimportant provided it is great enough to drive the limiting amplifier), then the output will be the product of the signal and the squared carrier above.

The final output is given by:

$$2A_m/\pi[\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t - 1/3\{\cos(\omega_m + 3\omega_c)t + \cos(\omega_m - 3\omega_c)t\} + 1/5\{\cos(\omega_m + 5\omega_c)t + \cos(\omega_m - 5\omega_c)t\} - 1/7\{\cos(\omega_m + 7\omega_c)t + \cos(\omega_m - 7\omega_c)t\} + \dots]$$

This output contains sum and difference frequencies of the signal and carrier, and of the signal and each of the odd harmonics of the carrier (in the ideal, perfectly balanced modulator, products of even harmonics are not present - in real modulators, which have residual offsets on their carrier ports, low-level even harmonic products are also present, just how low their level depends on the size of the offset). In most applications, a filter is used to remove the products of the higher harmonics so that, effectively, the modulator does behave like a multiplier. (In analyzing the above expressions, we must remember that  $\cos(A) = \cos(-A)$ , so that  $\cos(\omega_m - N\omega_c)t = \cos(N\omega_c - \omega_m)t$ , so we do not have to worry about "negative frequencies".) After filtering, the modulator output is given by:

$$2A_m/\pi[\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t]$$

Because of the  $2/\pi$  term, a modulator has a minimum 3.92dB insertion loss, in the absence of any gain. (The AD831 has a gain of 3.92dB to provide unity gain from RF to IF).

The most obvious application of a modulator is a *mixer* or *frequency changer*. If we apply an input signal at  $F_1$  and a carrier at  $F_2$  to a modulator, we find that the output contains signals at the sum and difference frequencies as shown in Figure 3.50. This applies even if the signal is a modulated signal containing a number of frequency components.



## THE MODULATOR AS A MIXER (FREQUENCY CHANGER)

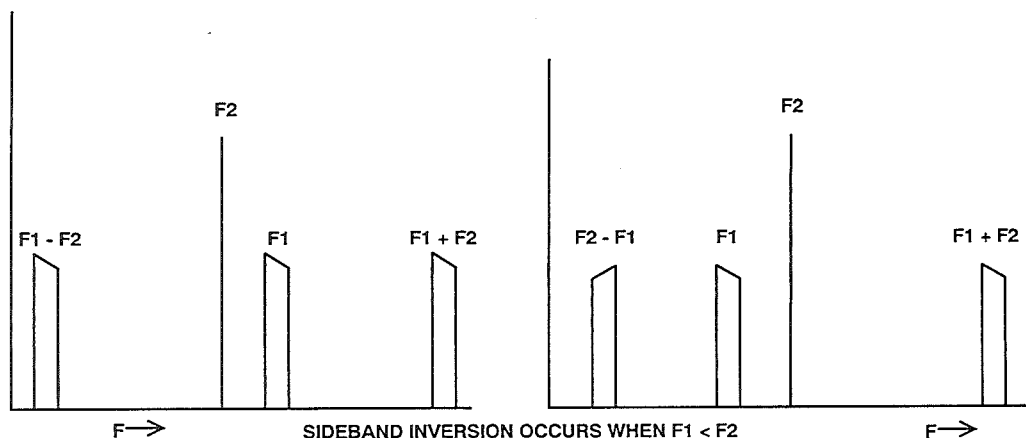


Figure 3.50

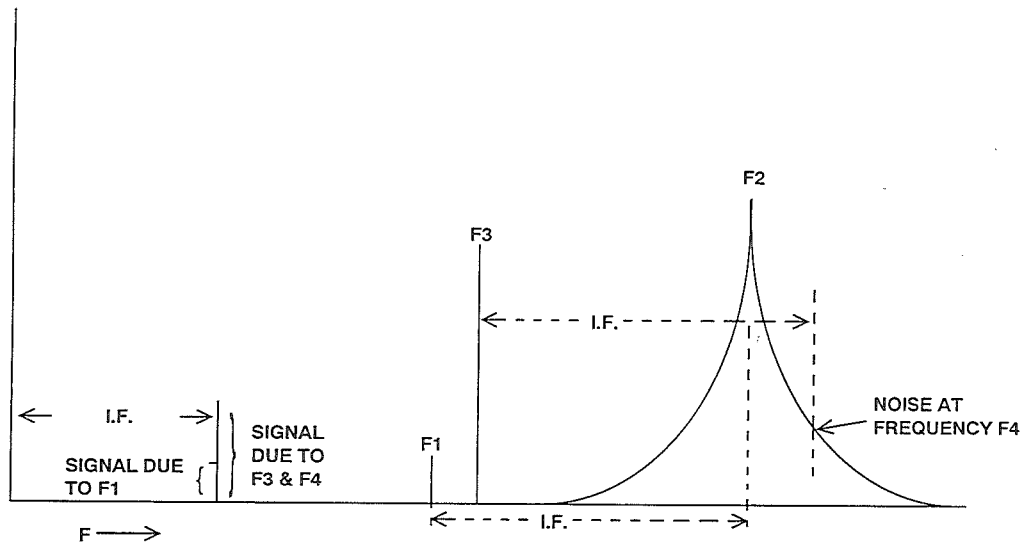
As we have mentioned above, we cannot have “negative frequencies”, and so if  $F1 - F2$  is negative, what we actually see is a frequency of  $F2 - F1$ . If  $F1$  is a complex signal containing a number of components, however, we find that if the carrier frequency,  $F2$ , is less than  $F1$ , then the sidebands are inverted in both the sum and difference products, but if  $F2$  is greater than  $F1$ , then in the difference product, the sidebands are inverted, as shown in the diagram.

The *mixer*, or frequency changer, is a key component in most radio receivers. While it is inappropriate to go into a detailed discussion of receiver design in this section, it is perhaps useful to point out two important features of modulators for use in receivers. These are *noise* and *strong signal performance* (see References 4 and 5).

Suppose that we have a mixer with a noisy carrier channel which causes the

carrier frequency,  $F2$ , to spread out on either side of its center as shown in Figure 3.51. If we are receiving a small wanted signal,  $F1$ , then we shall see a small IF output from the mixer at  $F2 - F1$ . If, however, there is a strong unwanted signal at  $F3$ , then the product,  $F4 - F3$ , of  $F3$  and that part of the broadband carrier noise indicated by  $F4$  on the diagram, will also fall at the IF and, being larger than the wanted IF component, will swamp it. This phenomenon is known as *reciprocal mixing*, and can cause severe limitation on the dynamic range of a receiver. While it is probably more commonly caused by noise or spurious synthesizer sidebands in the oscillator driving the modulator carrier port, it is common for it to be caused by noise in the modulator itself, and it should certainly be considered when choosing a mixer for radio receiver (see Reference 6).

## RECIPROCAL MIXING



NOTE: NOISE ON THE CARRIER PORT CAUSES UNWANTED RESPONSES

Figure 3.51

In the past, the sensitivity of a radio receiver has been one of its most important features. Today, while sensitivity is still important, the behavior of the receiver in the presence of strong signals is equally important. The characteristic chosen as a measure of a mixer's performance in this respect is its *third order intermodulation* performance. The key specification is the *third order intercept point*.

Consider a nonlinear amplifier with two large input signals, at  $F_1$  and  $F_2$  as

shown in Figure 3.52. The nonlinearity gives rise to additional output components at  $F_1 + F_2$  and  $F_1 - F_2$ : these are known as *second order intermodulation products*. These second order products mix with the original signals and produce *third order intermodulation products* at frequencies  $2F_1 - F_2$  and  $2F_2 - F_1$ .

## SECOND AND THIRD-ORDER INTERMODULATION PRODUCTS FOR $f_1 = 5\text{MHz}$ , $f_2 = 6\text{MHz}$

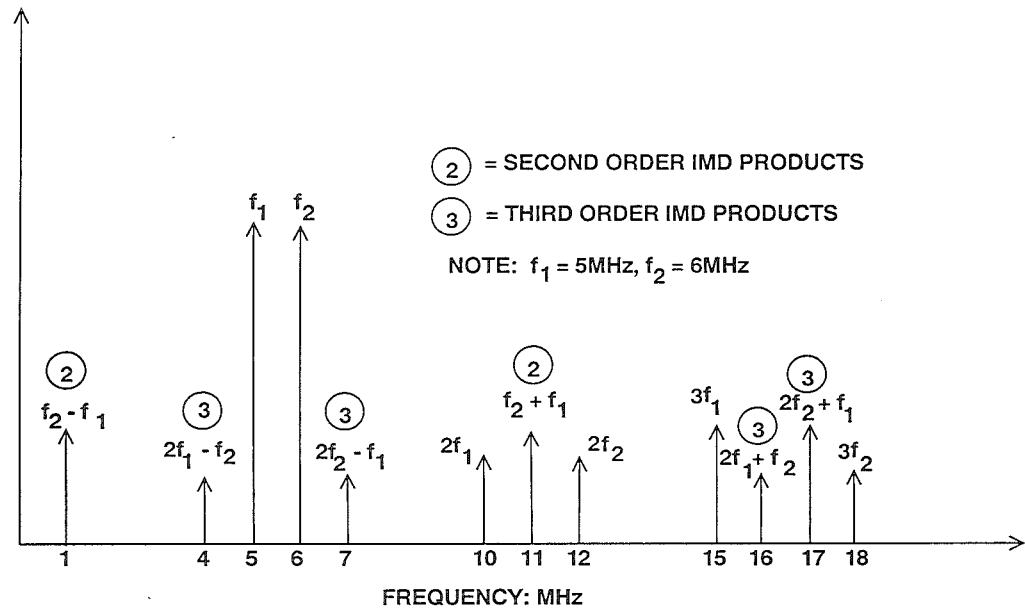


Figure 3.52

The third order intermodulation products are a major nuisance in radio reception, especially in channelized systems, because they fall close to the signals causing them. As an example, consider a receiver monitoring a frequency of 145.5000MHz. In Europe, this frequency is the calling frequency of the 2 meter Amateur Band. Working channels in this band are separated by 25kHz. Suppose that there are two transmitters working at 145.400 and 145.450 MHz respectively. The third order IMD products of these two frequencies fall at 145.350 and 145.500MHz. If the receiver is liable to third order IMD, it will respond to the third order products - which it itself produces - and appear to be receiving a signal at 145.500MHz.

It is impossible to design an amplifier or mixer which is unaffected by third order intermodulation. All that can be done is

to minimize the problem. The third order intercept point mentioned above is the parameter which measures how susceptible a device is to third order IMD.

If we plot the input versus the output amplitudes of an amplifier on a log/log (dB/dB) scale as shown in Figure 3.53, we obtain a straight line slope of unity. At a certain input level, the device saturates, and the output ceases to rise. A measure of this saturation point is known as the *1dB compression point*. If we plot the level of the second order IMD products in the output against the level of a two-tone input on the same axes, we obtain a straight line with a slope of 2. This line also ceases to rise when it reaches some limit. If, however, we extend the two straight lines past their limiting values, they will eventually cross. The value of the power in one of the two-tone inputs at this "inter-

cept point" is the *second order intercept point* of the device or system being measured. The level of the third order IMD products can also be plotted as a function of input, and the slope of the

straight line is 3. The intersection of this line with the extension of the unity-slope line is known as the *third order intercept point*.

## INTERCEPT POINTS, GAIN COMPRESSION, AND IMD

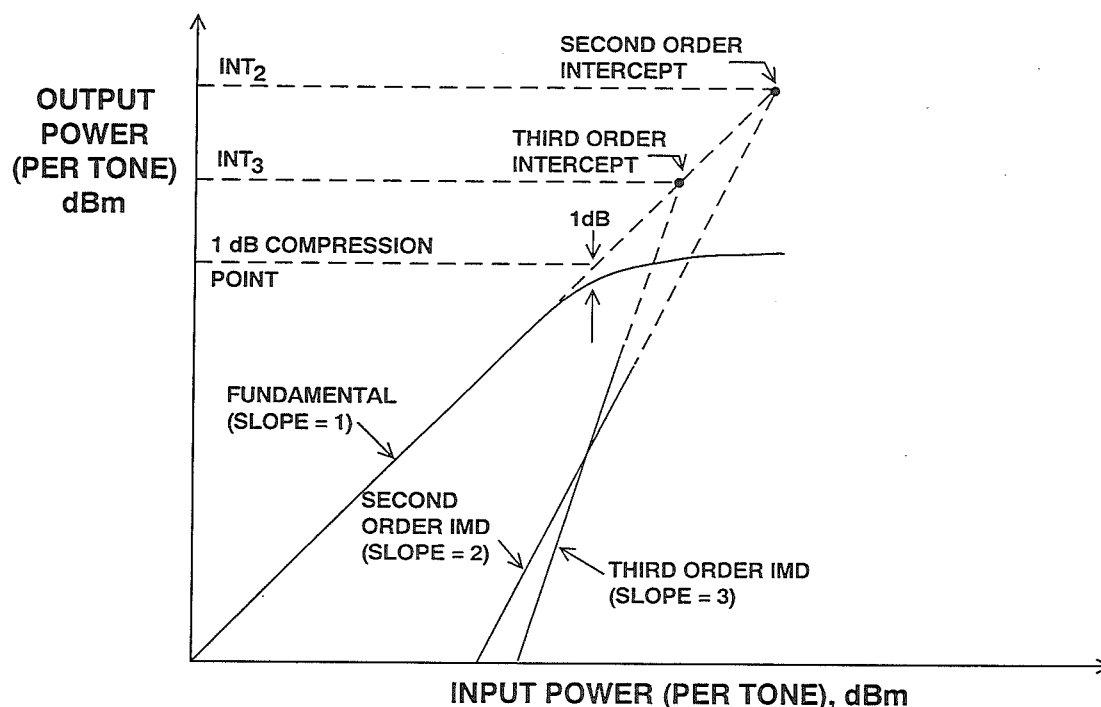


Figure 3.53

In mixers for receivers, values of third order intercept point can vary from  $-15\text{dBm}$  to over  $+45\text{dBm}$ . Any value below  $0\text{dBm}$  is generally considered poor, and good performance requires values of at least  $+15\text{dBm}$  and, preferably, more. The second-order intercept point may also be specified, but it is generally of less concern.

The AD831 is a low distortion, wide dynamic range, monolithic mixer for use in such applications as RF to IF down conversion in HF and VHF receivers, the second mixer in digital mobile radio base stations, direct-to-baseband conversion, quadrature modulation and

demodulation, and doppler-frequency shift detection in ultrasound imaging applications. The mixer includes a local oscillator driver and a low-noise output amplifier. The AD831 provides a  $+24\text{dBm}$  third-order intercept point for  $-10\text{dBm}$  local oscillator power, thus improving system performance and reducing system cost, compared to passive mixers, by eliminating the need for a high power local oscillator driver and its associated shielding and isolation problems. A simplified block diagram of the AD831 is shown in Figure 3.54, and key specifications in Figure 3.55.

## THE AD831 LOW DISTORTION MIXER

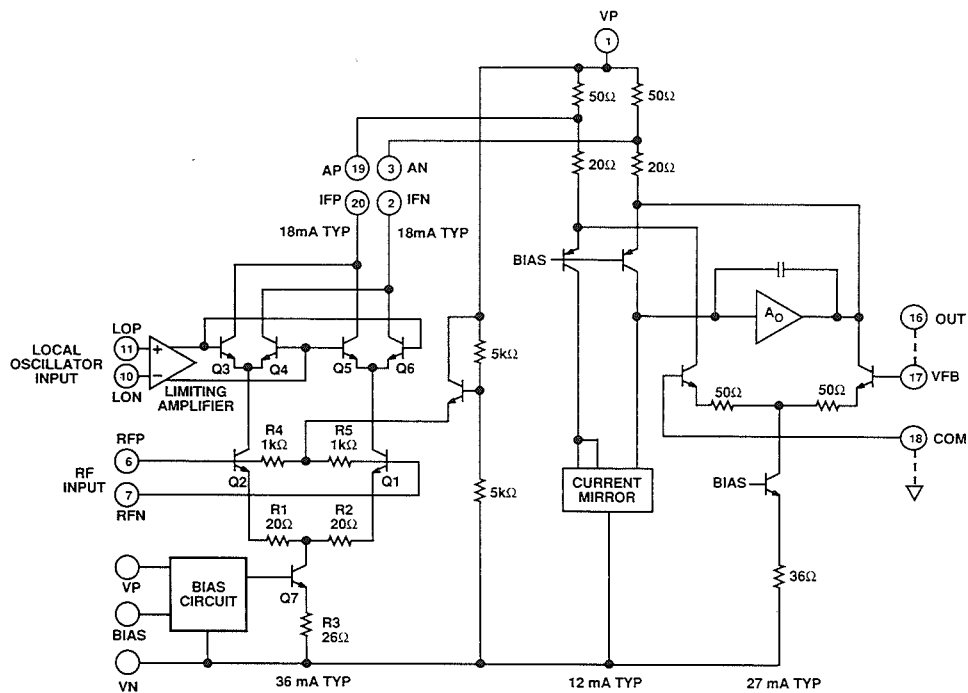


Figure 3.54

## AD831 MIXER KEY FEATURES

- **Doubly-Balanced Mixer**
- **Low Distortion:**
  - ◆ +24dBm Third Order Intercept
  - ◆ +10dBm 1dB Compression Point
- **Low LO Drive Required: -10dBm**
- **Bandwidth:**
  - ◆ 500MHz RF and LO Input Bandwidths
  - ◆ 250MHz Differential Current IF Output
  - ◆ DC to > 200MHz Single-Ended Voltage IF Output

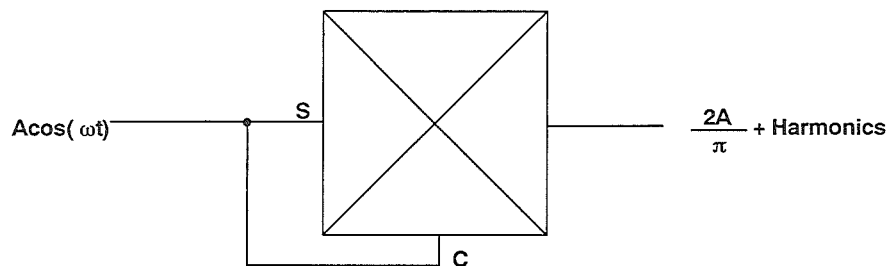
Figure 3.55

The basic mixing property of modulators is also used for many operations where dynamic range is far less important. These include frequency synthesis by mixing, frequency changing with fixed level signals, and sideband generation.

One application worth considering is using a modulator as a precision recti-

fier. If an AC signal is applied to both inputs of a modulator as shown in Figure 3.56, the instantaneous output will be equal to the input, if the input is positive, and to the inverse of the input (and therefore still positive), if the input is negative. This arrangement, therefore, behaves as a precision rectifier.

## A MODULATOR USED AS A PRECISION RECTIFIER



**Figure 3.56**

If, instead of applying a signal to both ports of a modulator, a signal is applied to the signal port and a reference signal at the same frequency (but not necessarily the same phase) to the carrier port, then the output will be propor-

tional both to the amplitude of the signal input and the cosine of their phase difference. In this mode a modulator acts as a phase-sensitive rectifier (see Figure 3.57).

## A MODULATOR USED AS A PHASE-SENSITIVE RECTIFIER

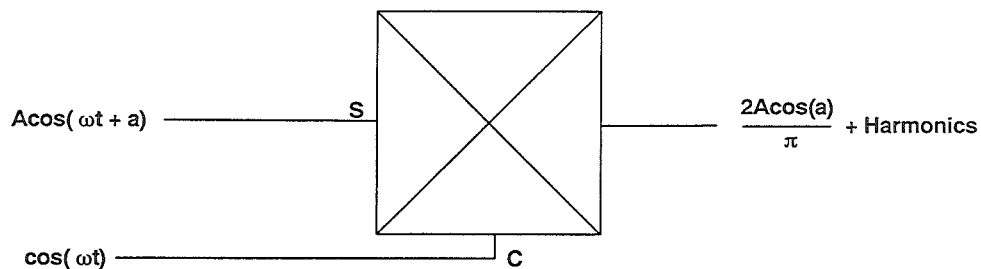


Figure 3.57

## AUTOMATIC GAIN CONTROL (AGC) AND VOLTAGE-CONTROLLED AMPLIFIERS (VCAs)

In radio systems, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic-range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1MHz carrier modulated at 1kHz to a 30% modulation depth would convey the same information, whether the received carrier level is at 0dBm or -120dBm. Some type of automatic gain control (AGC) in the receiver is generally utilized to restore the carrier amplitude to some normalized reference level, in the presence of large input fluctuations.

AGC circuits are dynamic-range compressors which respond to some metric of the signal – often its mean amplitude – acquired over an interval corresponding to many periods of the carrier. Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since impulsive noise can now activate the AGC detection circuits. Nonlinear filtering and the concept of “delayed AGC” can be useful in optimizing an AGC system. Many tradeoffs are found in practice; Figure 3.58 shows a basic system.

## A TYPICAL AUTOMATIC GAIN CONTROL (AGC) SYSTEM)

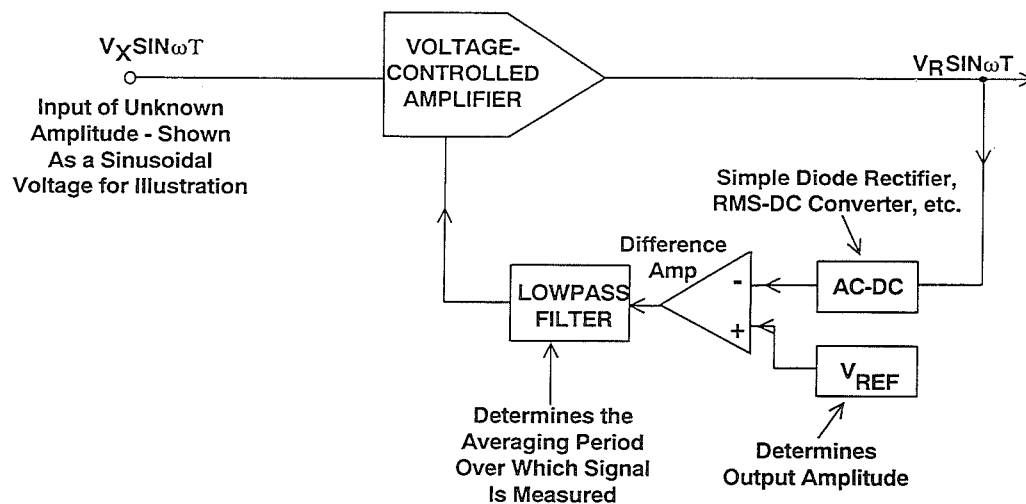


Figure 3.58

It is interesting to note that an AGC loop actually has two outputs. The obvious output is the amplitude-stabilized signal. The less obvious output is the control voltage to the VCA, which is

in reality, a measure of the average amplitude of the input signal. If the system is precisely scaled, the control voltage may be used as a measure of the input signal.



## VOLTAGE CONTROLLED AMPLIFIERS (VCAs)

A multiplier can be used as a variable-gain amplifier as shown in Figure 3.59. The control voltage is applied to one input, and the signal to the other. The AD539 two-quadrant multiplier (60MHz bandwidth) and the AD844 current feedback amplifier can be used in a 20MHz variable gain amplifier configuration (Figure 3.60). The frequency response of the variable gain amplifier for gains of +4 to -46dB, as

well as the transient response, is shown in Figure 3.61. A current feedback (or transimpedance) amplifier is ideally suited for this application, since its bandwidth remains relatively constant over a wide range of closed-loop gains. In this configuration, the gain is directly proportional to the control voltage. The transfer function of the circuit is

$$V_w = -\frac{V_x V_y}{2V}$$

3

### USING A MULTIPLIER AS A VOLTAGE-CONTROLLED-AMPLIFIER (VCA)

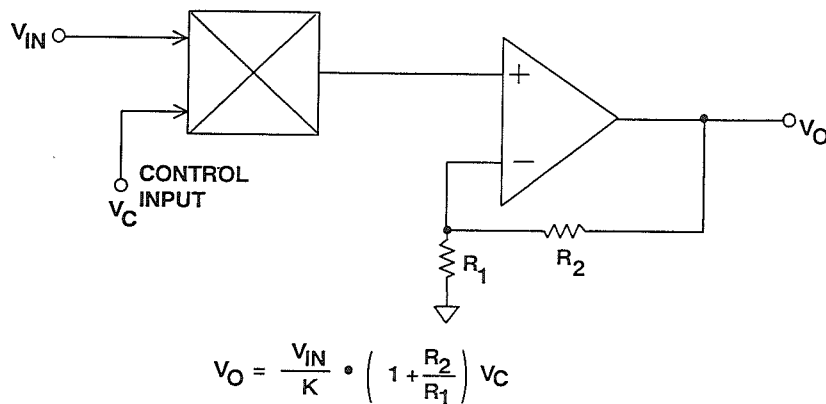


Figure 3.59

# A 20MHz VCA USING THE AD539 MULTIPLIER AND THE AD844 CURRENT FEEDBACK OP AMP

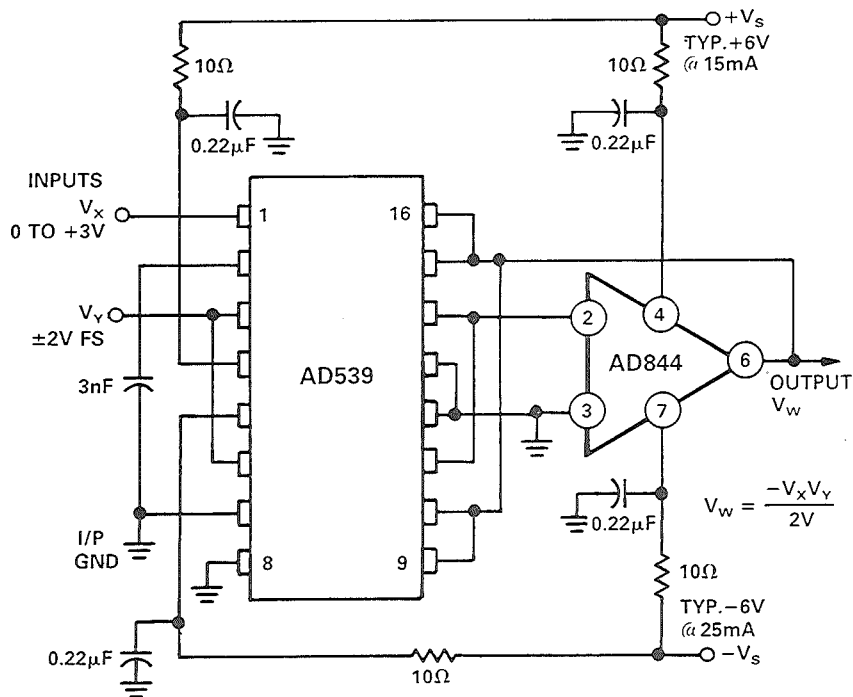
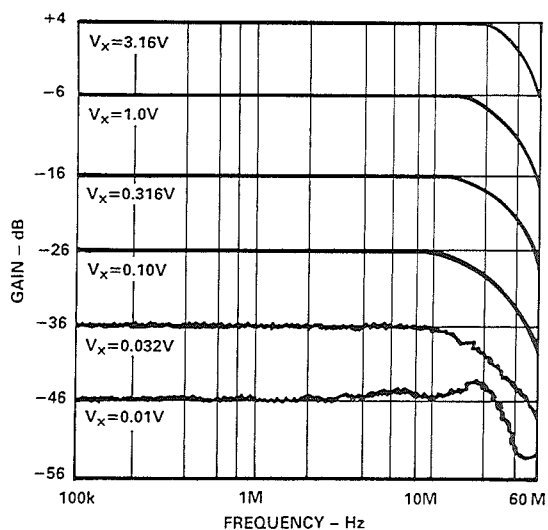
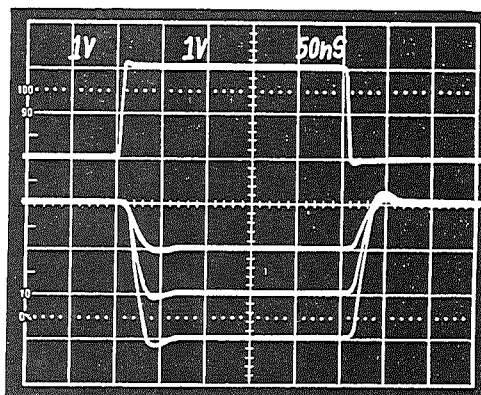


Figure 3.60

## FREQUENCY AND TRANSIENT RESPONSE OF THE 20MHz VCA



VGA ac Response



VGA Transient Response with  
 $V_x = 1V, 2V, \text{ and } 3V$

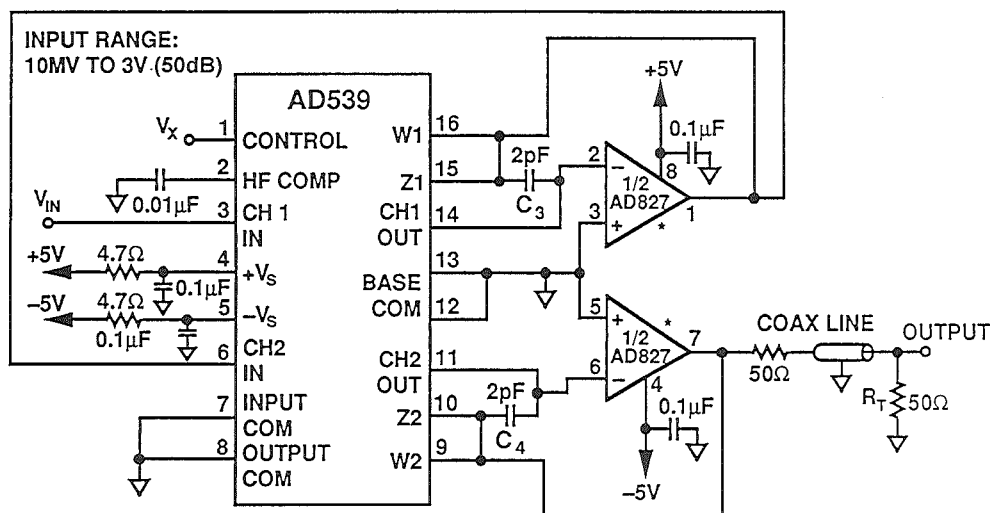
Figure 3.61

In Figure 3.62, the AD827 dual high-speed op-amp is used to provide output current-to-voltage conversion, and the two sections of the AD539 multiplier are connected in series to provide a VCA with a square-law response. The trans-

fer function of this circuit (measured at the reverse-terminated load) is

$$\frac{V_{out}}{V_{in}} = \frac{V_x^2}{8V^2}$$

### AN 8MHz VCA WITH SQUARE-LAW GAIN CONTROL USING THE AD539 MULTIPLIER



\*PINOUT SHOWN IS FOR MINI-DIP PACKAGE

$$V_{out} \text{ AT TERMINATION RESISTOR, } R_T = V_x^2 V_{in} / 8V^2$$

$$V_{out} \text{ AT PIN 7 OF AD827} = V_x^2 V_{in} / 4V^2$$

Figure 3.62

Alternately, the two sections of the AD539 may be operated in parallel with linear gain control. The frequency response of this circuit is about 8MHz using the AD827 op amp. The AD811 high-speed op amp may be substituted in these circuits for increased performance.

Faster op-amps and faster multipliers may be used to achieve higher bandwidth VCAs. A 90MHz VCA is shown in Figure 3.63. The AD834's outputs are in the form of differential currents from a

pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500MHz) is available. In this case, more moderate bandwidth is obtained using current-to-voltage conversion provided by the AD811 op amp, to realize a practical amplifier with a single-ended, ground-referenced output. Using feedback resistors  $R_8$  and  $R_9$  of  $511\Omega$ , the overall gain ranges from -70dB for  $V_G \sim 0$  to +12dB (a numerical gain of four) when  $V_G = +1V$ . The frequency response for the VCA is shown in Figure 3.64.

## A 90MHz VCA USING THE 500MHz AD834 MULTIPLIER AND THE AD811 OP AMP PROVIDES 80dB DYNAMIC RANGE

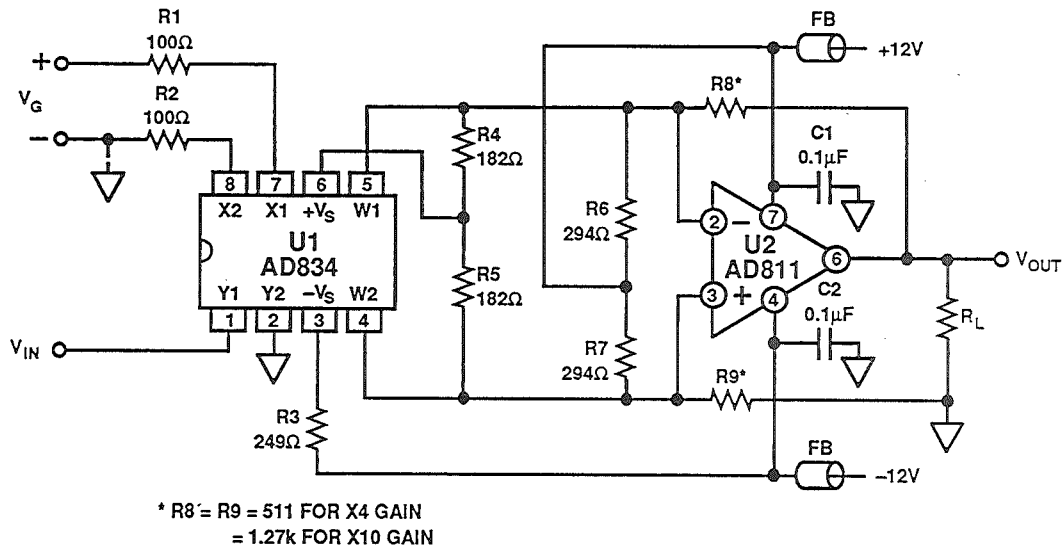


Figure 3.63

## FREQUENCY RESPONSE OF THE 90MHz VCA FOR MAXIMUM GAINS OF +12dB AND +20dB

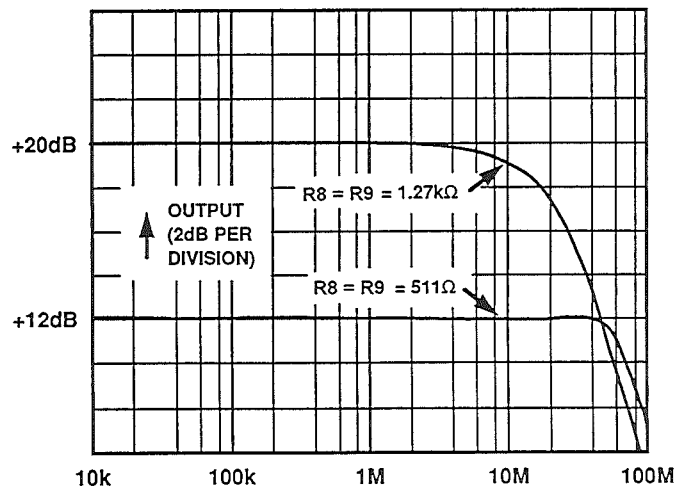


Figure 3.64

Most VCAs made with analog multipliers have gain which is *linear in volts* with respect to the control voltage, moreover they tend to be noisy. There is a demand, however, for a VCA which combines a wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, *linear-in-dB* gain. The AD600, AD602, and AD603 achieve these demanding and conflicting objectives with a unique and elegant solution - the X-AMP™ (for *exponential amplifier*). The concept is simple: a fixed-gain

amplifier follows a passive, broadband attenuator equipped with special means to alter its attenuation under the control of a voltage (see Figure 3.65). The amplifier is optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (about 30 to 40dB) and minimize distortion. Since this amplifier's gain is fixed, so also are its ac and transient response characteristics, including distortion and group delay; since its gain is high, its input is never driven beyond a few millivolts. Therefore, it is always operating within its small signal response range.

### SINGLE CHANNEL OF THE DUAL 30MHz AD600/AD602 X-AMP

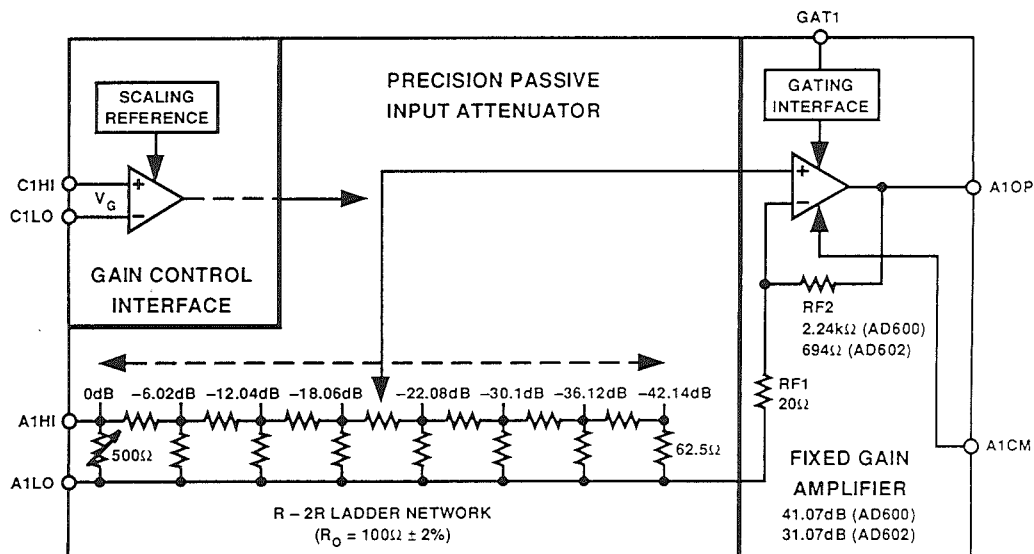


Figure 3.65

The attenuator is a 7-section (8-tap) R-2R ladder network. The voltage ratio between all adjacent taps is exactly 2, or 6.02dB. This provides the basis for the precise linear-in-dB behavior. The overall attenuation is 42.14dB. As will be shown, the amplifier's input can be connected to any one of these taps, or even *interpolated* between them, with only a small deviation error of about  $\pm 0.2$ dB. The overall gain can be varied all the way from the fixed (maximum) gain to a value 42.14dB less. For example, in the AD600, the fixed gain is 41.07dB (a voltage gain of 113); using this choice, the full gain range is -1.07dB to +41.07dB. The gain is

related to the control voltage by the relationship  $G_{dB} = 32V_G + 20$  where  $V_G$  is in volts. For the AD602, the fixed gain is 31.07dB (a voltage gain of 35.8), and the gain is given by  $G_{dB} = 32V_G + 10$ .

The gain at  $V_G = 0$  is laser trimmed to an absolute accuracy of  $\pm 0.2$ dB. The gain scaling is determined by an on-chip bandgap reference (shared by both channels), laser trimmed for high accuracy and low temperature coefficient. Figure 3.66 shows the gain versus the differential control voltage for both the AD600 and the AD602.

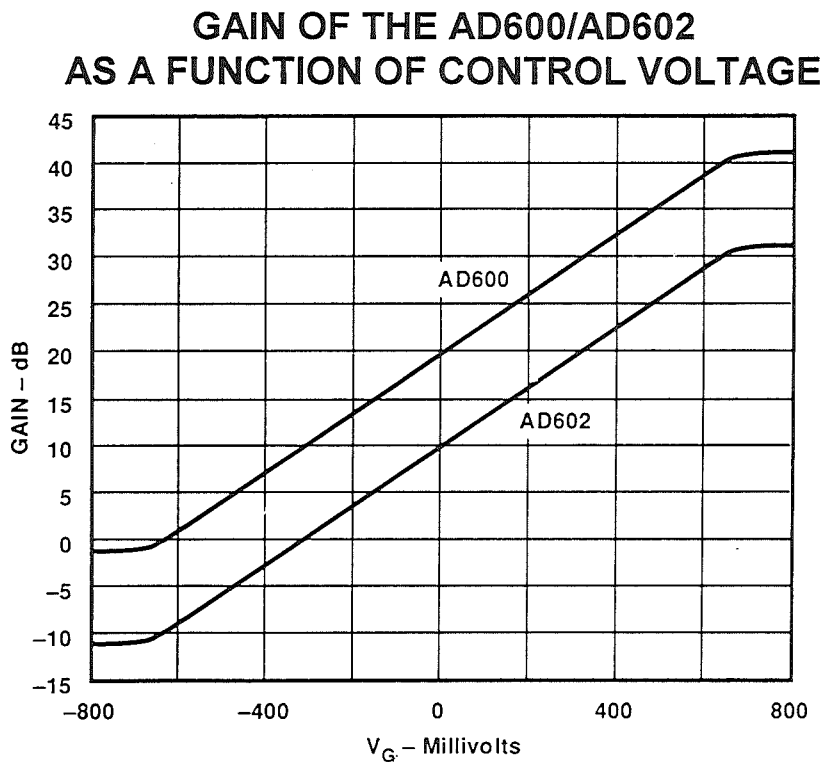


Figure 3.66

In order to understand the operation of the AD600/AD602, consider the simplified diagram shown in Figure 3.67. Notice that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance ( $g_m$ ) stages; the other input of all these  $g_m$

stages is connected to the amplifier's gain-determining feedback network,  $R_{F1}/R_{F2}$ . When the emitter bias current,  $I_E$ , is directed to one of the 8 transistor pairs (by means not shown here), it becomes the input stage for the complete amplifier.

3

### CONTINUOUS INTERPOLATION BETWEEN TAPS IN THE X-AMP IS PERFORMED WITH CURRENT-CONTROLLED $g_m$ STAGES

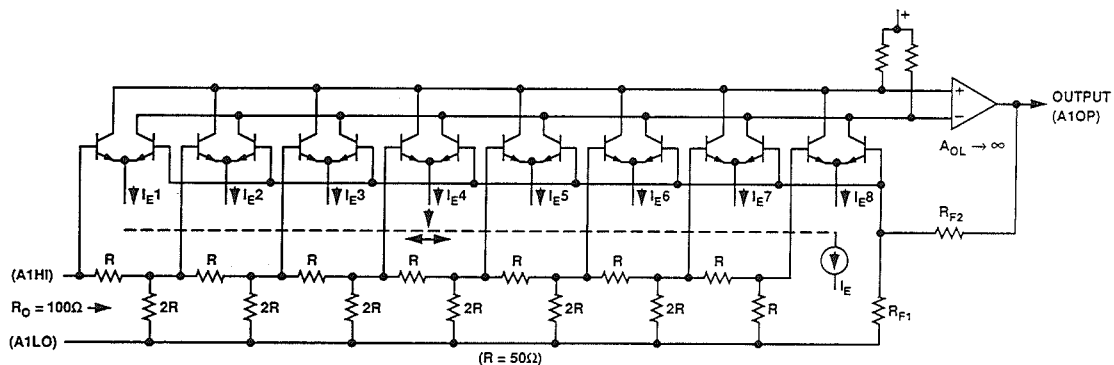


Figure 3.67

When  $I_E$  is connected to the pair on the left-hand side, the signal input is connected directly to the amplifier, giving the maximum gain. The distortion is very low, even at high frequencies, due to the careful open-loop design, aided by the negative feedback. If  $I_E$  were now to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02dB, and the distortion would remain low, because only one  $g_m$  stage remains active.

In reality, the bias current is *gradually* transferred from the first pair to the second. When  $I_E$  is equally divided between two  $g_m$  stages, both are active, and the situation arises where we have an op amp with two input stages fighting for control of the loop, one getting the full signal, and the other getting a signal exactly half as large.

Analysis shows that the effective gain is reduced, not by 3dB, as one might first

expect, but rather by  $20\log 1.5$ , or 3.52dB. This error, when divided equally over the whole range, would amount to a gain ripple of  $\pm 0.25\text{dB}$ ; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of  $I_E$  always flows in adjacent stages. This smoothes the gain function and actually lowers the ripple (see Reference 12). As  $I_E$  moves further to the right, the overall gain progressively drops.

The total input-referred noise of the X-AMP™ is  $1.4\text{nV}/\sqrt{\text{Hz}}$ ; only slightly more

than the thermal noise of a  $100\Omega$  resistor which is  $1.29\text{nV}/\sqrt{\text{Hz}}$  at  $25^\circ\text{C}$ . The input-referred noise is constant regardless of the attenuator setting, therefore the output noise is always constant and independent of gain. For the AD600, the amplifier gain is 113 and the output noise spectral density is therefore  $1.4\text{nV}/\sqrt{\text{Hz}} \times 113$ , or  $158\text{nV}/\sqrt{\text{Hz}}$ . Referred to its maximum output of 2V rms, the signal-to-noise ratio would be 82dB in a 1MHz bandwidth. The corresponding signal-to-noise ratio of the AD602 is 10dB greater, or 92dB. Key features of the AD600/AD602 are summarized in Figure 3.68.

## KEY FEATURES OF THE AD600/AD602 X-AMPS

- Precise Decibel-Scaled Gain Control
- Accurate Absolute Gain Calibration
- Low Input-Referred Noise ( $1.4\text{nV}/\sqrt{\text{Hz}}$ )
- Constant Bandwidth (dc to 35MHz)
- Low Distortion:  $-60\text{dBc}$  THD at  $\pm 1\text{V}$  Output
- Stable Group Delay ( $\pm 2\text{ns}$  Over Gain Range)
- Response Time: Less than  $1\mu\text{s}$  for 40dB Gain Change
- Low Power (125mW per channel maximum)
- Differential Control Inputs

Figure 3.68

The AD603 X-AMP is a single version of the AD600/AD602 which provides 90MHz bandwidth. There are two pin-programmable gain ranges:  $-11\text{dB}$  to

$+31\text{dB}$  with 90MHz bandwidth, and  $+9\text{dB}$  to  $+51\text{dB}$  with 9MHz bandwidth. Key specifications for the AD603 are summarized in Figure 3.69.



## KEY FEATURES OF THE AD603 X-AMP

- Precise "Linear in dB" Gain Control
- Pin Programmable Gain Ranges:
  - 11dB to +31dB with 90MHz Bandwidth
  - +9dB to + 51dB with 9MHz Bandwidth
- Bandwidth Independent of Variable Gain
- Low Input-Referred Noise ( $1.3\text{nV}/\sqrt{\text{Hz}}$ )
- $\pm 0.5\text{dB}$  Typical Gain Accuracy
- Low Distortion:  $-60\text{dBc}$ , 1V rms Output @ 10MHz
- Low Power (125mW)
- 8-pin Plastic SOIC or Ceramic DIP

3

Figure 3.69

## AN 80 dB RMS-LINEAR-dB MEASUREMENT SYSTEM

Monolithic RMS/DC converters provide an inexpensive means to measure the rms value of a signal of arbitrary waveform. They also may provide a low-accuracy logarithmic ("decibel-scaled") output. However, they have a fairly small dynamic range – typically only 50dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3dB bandwidth of 900kHz for an input of 100mV rms, but only a 100kHz bandwidth for an input of 10mV rms. Its "raw" logarithmic output is unbuffered, uncalibrated, and not stable over temperature, requiring considerable support circuitry, including at least two adjustments and a special high-TC resistor.

All of these problems can be eliminated using an AD636 merely as *the detector element* in an AGC loop, in which the difference between the rms output of the amplifier and a fixed DC reference is nulled in a loop integrator. The dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the RMS/DC converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal-dependent. If the amplifier has a precise exponential ("linear-dB") gain-control law, its control voltage is forced by the AGC loop to have the general form

$$V_{\text{LOG}} = V_S \log_{10} \frac{V_{\text{IN(RMS)}}}{V_Z}$$

where  $V_S$  is the logarithmic slope and  $V_Z$  is the logarithmic intercept, that is, the value of  $V_{\text{IN}}$  for which  $V_{\text{LOG}}$  is zero.

Figure 3.70 shows a practical wide-dynamic-range rms measurement system using the AD600. It can handle inputs of from 100 $\mu$ V to 1V rms (4 decades) with a constant measurement

bandwidth of 20Hz to 2MHz, limited primarily by the AD636 RMS/DC converter. Its logarithmic output is a buffered voltage, accurately-calibrated to 100mV/dB, or 2V per decade, which simplifies the interpretation of the reading when using a DVM, and is arranged to be -4V for an input of 100 $\mu$ V rms input, zero for 10mV, and +4V for a 1V rms input. In terms of the above equation,  $V_S$  is 2V and  $V_Z$  is 10mV.

## A COMPLETE 80dB RMS-LINEAR-dB MEASUREMENT SYSTEM

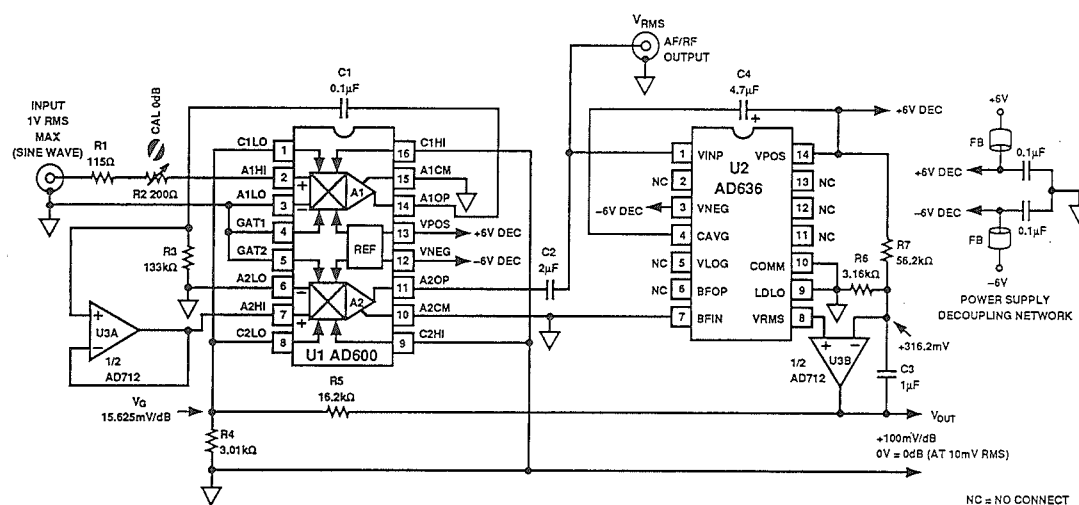


Figure 3.70

Note that the peak "log-output" of  $\pm 4$ V requires the use of  $\pm 6$ V supplies for the dual op-amp U3 (AD712), although lower supplies would suffice for the AD600 and AD636. If only  $\pm 5$ V supplies are available, it will either be necessary to use a reduced value for  $V_S$  (say, 1V,

in which case the peak output would be only  $\pm 2$ V), or to restrict the dynamic range of the signal to about 60dB.

The two amplifiers of the AD600 are used in cascade. The modest bandwidth of the unity-gain buffer U3A eliminates

the risk of instability at the highest gains. The buffer also allows the use of a high-impedance coupling network (C1/R3) which introduces a high-pass corner at about 12Hz. An input attenuator of 10dB ( $\times 0.316$ ) is now provided by R1 + R2 operating in conjunction with the AD600's input resistance of 100 $\Omega$ . The adjustment provides exact calibration of  $V_Z$  in critical applications, but R1 and R2 may be replaced by a fixed resistor of 215 $\Omega$  if very close calibration is not needed, since the input resistance of the AD600 (and all the other key parameters of it and the AD636) are already laser-trimmed for accurate operation. This attenuator allows inputs as large as  $\pm 4V$  to be accepted, that is, signals with an rms value of 1V combined with a crest-factor of up to 4.

The output of A2 is AC-coupled via another 12Hz high-pass filter formed by C2 and the 6.7k $\Omega$  input resistance of the AD636. The averaging time-constant for the RMS/DC converter is determined by C4. The unbuffered output of the AD636 (at pin 8) is compared with a fixed voltage of +316mV set by the positive supply voltage of +6V and resistors R6 and R7. ( $V_Z$  is proportional to this voltage, and systems requiring greater calibration accuracy should replace the supply-dependent reference with a more stable source. However,  $V_S$  is independent of the supply voltages, being determined by the band-gap reference in the X-AMP.) Any difference in these voltages is integrated by the op-amp U3B, with a time-constant of 3ms formed by the parallel sum of R6/R7 and C3.

If the gain of the AD600 is too high,  $V_{OUT}$  will be greater than the "set-point" of 316mV, causing the output of

U3B – that is,  $V_{LOG}$  – to ramp up (note that the integrator is non-inverting). A fraction of  $V_{LOG}$  is connected to the *inverting* gain-control inputs of the AD600, causing the gain to be reduced, as required, until  $V_{OUT}$  is equal to 316mV (DC), at which time the AC voltage at the output of A2 is forced to exactly 316mV (rms). This fraction is set by R4 and R5 such that a 15.625mV change in the control voltages of A1 and A2 – which would change the gain of the two cascaded amplifiers by 1 dB – requires a change of 100mV at  $V_{LOG}$ . Since A2 is forced to operate well below its limiting level, waveforms of high crest-factor can be tolerated throughout the amplifier.

To verify the operation, assume an input of 10mV rms is applied to the input, resulting in a voltage of 3.16mV rms at the input to A1 (due to the 10dB attenuator). If the system performs as claimed,  $V_{LOG}$  (and hence  $V_G$ ) should be zero. This being the case, the gain of both A1 and A2 will be 20dB and the output of the AD600 will be 100 times (40dB) greater than its input, 316mV rms. This is the input required at the AD636 to balance the loop, confirming the basic operation. Note that unlike most AGC circuits, (which often have a high gain/temperature coefficient due to the internal "kT/q" scaling), the voltages and thus the output of this measurement system are very stable over temperature. This behavior arises directly from the exact exponential calibration of the ladder attenuator.

Typical results are shown for a sinewave input at 100kHz. Figure 3.71 shows that the output is held very close to the set-point of 316mV rms over an input range in excess of 80dB.

## SIGNAL OUTPUT $V_{out}$ VERSUS INPUT LEVEL

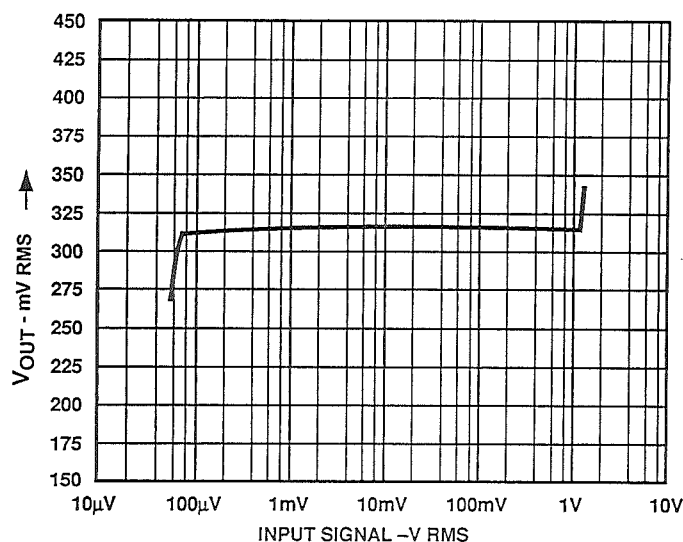


Figure 3.71

Figure 3.72 shows the “decibel” output voltage,  $V_{LOG}$ , and Figure 3.73 shows that the *deviation* from the ideal output

logarithmic output is within  $\pm 1$  dB for the 80dB range from 80  $\mu$ V to 800mV.

## THE LOGARITHMIC OUTPUT $V_{LOG}$ VERSUS INPUT SIGNAL LEVEL

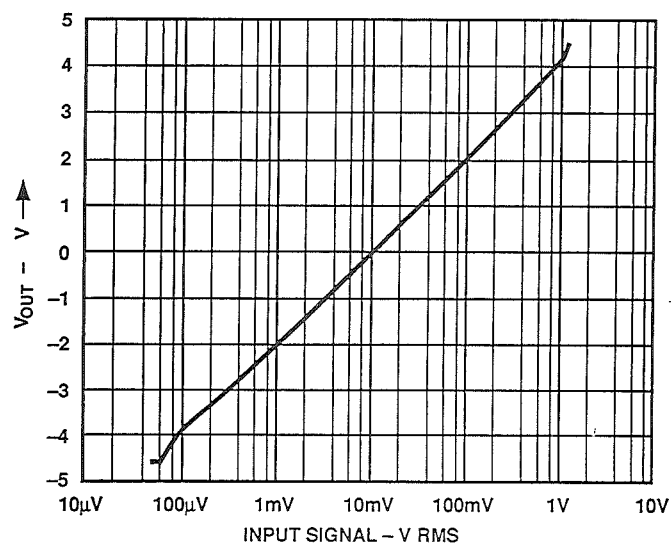


Figure 3.72

### DEVIATION FROM THE IDEAL LOGARITHMIC OUTPUT

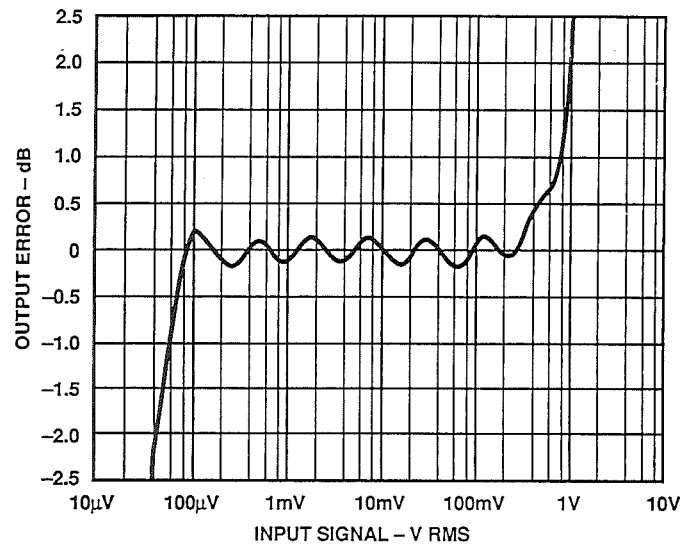


Figure 3.73

By suitable choice of the input attenuator,  $R1+R2$ , this could be centered to cover any range from  $25\mu\text{V}$  to  $250\text{mV}$  to, say,  $1\text{mV}$  to  $10\text{V}$ , with appropriate correction to the value of  $V_Z$ . (Note that  $V_Z$  is not affected by the changes in the range). The gain ripple of  $\pm 0.2\text{dB}$  seen in this curve is the result of the finite interpolation error of the X-AMP. It occurs with a periodicity of  $12\text{dB}$  – twice the separation between the tap points in each amplifier section.

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a  $3\text{dB}$  offset between the

two pairs of control voltages. A simple means to achieve this is shown in Figure 3.74: the voltages at  $C1\text{HI}$  and  $C2\text{HI}$  are “split” by  $\pm 46.875\text{mV}$ , or  $\pm 1.5\text{dB}$ . Alternatively, either one of these pins can be individually offset by  $3\text{dB}$ , and a  $1.5\text{dB}$  gain adjustment made at the input attenuator ( $R1+R2$ ). The error curve shown in Figure 3.75 demonstrates that over the central portion of the range, the output voltage can be maintained very close to the ideal value. The penalty for this modification is higher errors at both ends of the range.

## METHOD FOR CANCELING THE GAIN-CONTROL RIPPLE

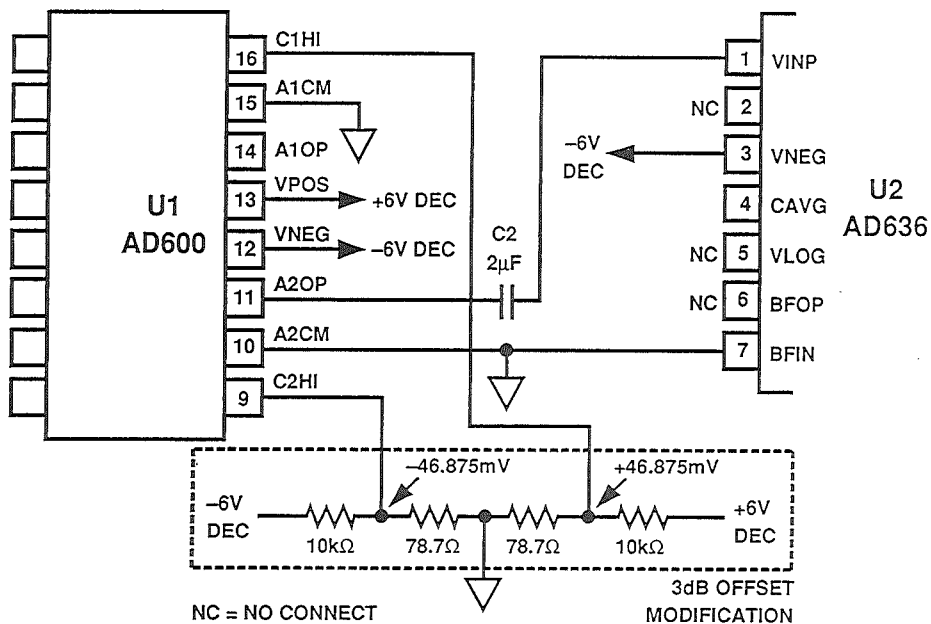


Figure 3.74

## LOGARITHMIC ERROR USING THE PREVIOUS CIRCUIT MODIFICATION

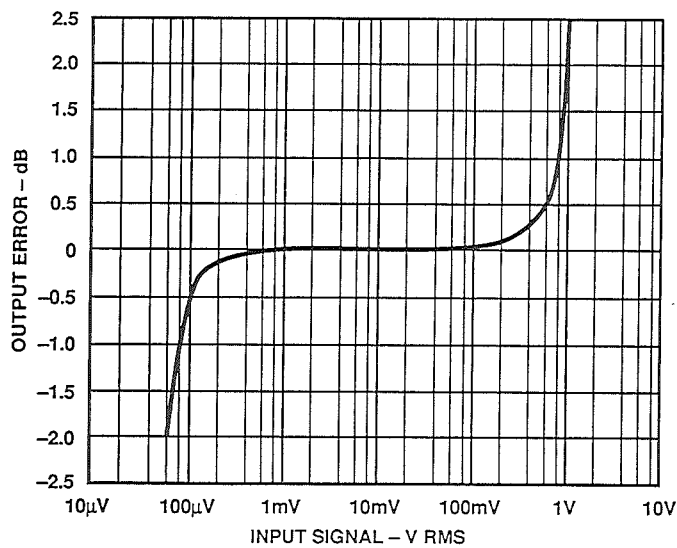


Figure 3.75

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